MOS & SPECIAL COS/MOS
2nd EDITION
ISSUED MARCH 1981

INTRODUCTION

This databook contains data sheets on the SGS-ATES range of products in MOS and COS/MOS technology.
The information on each product has been specially presented in order that the performance of the product can be readily evaluated within any required equipment design.
The databook also contains a summary of the processes available in SGS-ATES for the development and production of the products listed.

NUMERICAL INDEX

FUNCTIONAL INDEX

FUNCTIONAL INDEX (continued)

MOS PROCESSES AND PRODUCTS

N-channel is the major MOS process at SGS. This process was developed independantly and has significant advantages, but it remains compatible for production of true second source products. Current production uses 5 μm and 4 μm features for products such as the M3870, Z8, Z80 and Z8000 microprocessors, 16K and 64K ROMs.

The SGS NV-RAM (Non-volatile memory) process which is compatible with the N-channel process allows integration of non-volatile memory blocks on the same chip as other random logic. This NV-RAM process provides better reliability than competitive MNOS products and an extrapolated data retention of over 100 years. Products using this compatible process include the M120 256x4 non-volatile RAM, the 16 and 32 channel Electronic Program Memories for voltage synthesised TV tuning, a new Phase Locked Loop and 32 word x 16 bit NV-RAM tuning circuit and the XCARD electronic credit card: this type of electronic credit card is forecast to replace existing magnetic cards and open up new markets in credit based POS applications.

THE TECHNOLOGY

Circuit design and layout on graphic terminals includes direct on-screen design for LSI products, advanced design rule check and process electrical layout check. Master mask production from the computer tapes is by automated electron beam exposure which eliminates the step-and-repeat mask production stage. Projection lithography machines are used for wafer exposure to extend working mask life and reduce defects. Ion implant, is used extensively for deposition and an Arsenic ion implant is planned for high speed circuits.

LOW VOLTAGE AND HIGH DENSITY CMOS

Three advanced technologies are in production at SGS: a Low Voltage Aluminium Gate process used for telephone MF and loop disconnect diallers, a High Density silicon gate process used for CODEC and TV remote control products and a High Density Low Voltage silicon gate process, operating on 1.5-2V supplies, aimed at pacemakers, microprocessors etc. The HD CMOS process, using a 4 μm technology increases random logic gate density by a factor of 4 and gives a 0.1 pJ power/speed performance which exceeds that of HMOS 2μm devices.

TELECOMMUNICATIONS CMOS

CMOS is a major technology for Telecommunications products. The speed/performance of High Density circuits closely matches the applications such as telephone diallers, tone ringers, CODEC's and cross point switches. The digital filters and analogue circuits integrated on the Multifrequency Tone Dialler chips provide a clean tone output meeting worldwide specifications. The low power consumption and high output drive allows a tone ringer to drive a transducer directly from the telephone line, the circuit uses a digital filter to detect the ringing tone from the line. The CMOS CODEC circuits integrate both analogue and digital blocks of the CODEC function and use little power.

SGS-ATES MOS PROCESSES

1. Low threshold N-channel enhancement/depletion mode with an N-type polycrystalline silicon gate
   - Threshold voltage: 0.6 to 1.2V
   - Supply voltage: V_{CC}= +5V
   - Used in static and dynamic systems (Z80/M3870/M36000)
   - Compatible with bipolar circuits

2. N-channel enhancement/depletion mode with an N-type polycrystalline silicon gate
   - Threshold voltage: 0.8 to 1.2V
   - Supply voltages: V_{DD}= +12V, V_{CC}= 5V
   - Used in static and dynamic systems
   - Compatible with bipolar circuits

3. N-channel enhancement/depletion mode with double N-type polycrystalline silicon gate
   - Threshold voltage: 0.8 to 1.2V with V_{BB}= -5V
   - Supply voltages: V_{DD}= +12V, V_{BB}= -5V, V_{CC}= 5V
   - Used for dynamic RAMs
   - Compatible with bipolar circuits

4. N-channel enhancement/depletion mode with double N-type polycrystalline silicon gate
   - Threshold voltage: 0.8 to 1.2V
   - Supply voltage: V_{CC}= 5V
   - Used for UV erasable and electrically programmable ROMs (M2716)
   - Compatible with bipolar circuits

5. N-channel enhancement/depletion mode with double N-type polycrystalline silicon gate
   - Threshold voltage: 0.8V to 1.2V
   - Supply voltages: V_{DD}= +12V, V_{CC}= +5V
   - Used for NON VOLATILE RAMs (M120/M193/M293)
   - Compatible with bipolar circuits

6. COS/MOS Aluminum Gate A & B process
   - Threshold voltage: 1 to 2V
   - Supply voltage: V_{DD}= +3 to +18V

7. COS/MOS Aluminum Gate - low threshold voltage
   - Threshold voltage: 0.5V to 1V
   - Supply voltage: V_{DD}= 1.5 to 5V

8. COS/MOS Silicon Gate High Density
   - Threshold voltage: 0.8V to 1.2V
   - Supply voltages: V_{DD}= +3 to 12V

DATA-SHEETS

MOS INTEGRATED CIRCUITS

M 054
M 055

1 OF 16 DECODER

- SPECIFICALLY DESIGNED FOR TV APPLICATION
- MINIMIZATION OF THE EXTERNAL COMPONENTS
- INTERNAL PULL-UP FOR USE WITH LIGHT PRESSURE SWITCHES (M054)
- OPEN DRAIN OUTPUTS FOR TOUCH CONTROL (M055)

The M 054, M 055 are monolithic integrated circuits specifically designed to act as interface between M 1025 (30 channel ultrasonic receiver) and H 580/590 (quad analog switch) in TV applications. The inputs A,B,C,D,E are driven directly from the corresponding outputs of the M 1025. If G input is high the circuits decode the binary combinations from 0 to 15, if G is low the combinations from 16 to 31 are decoded instead. The M 054 has an internal pull-up circuit on the outputs to minimize the number of external components when light pressure switches are used. The M 055 has open drain outputs for touch control applications. The circuits are constructed with N-channel silicon gate technology and are supplied in a 24-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to 20	V
$V_{O(off)}$	Off state output voltage (M 055 type)	20	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

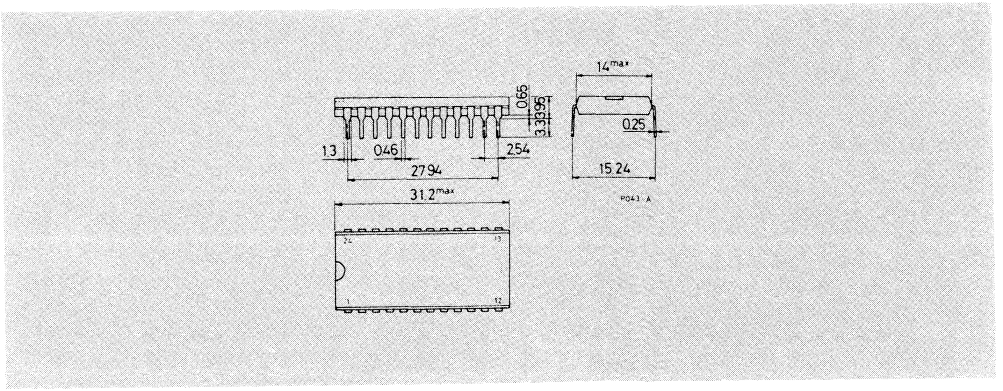
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages values are refered to V_{SS} pin voltage.

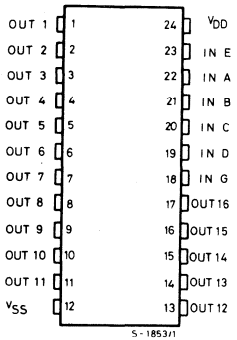
ORDERING NUMBERS: M 054 B1
M 055 B1

MECHANICAL DATA

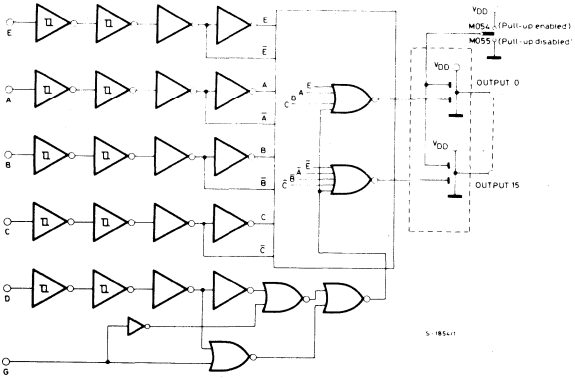
Dimensions in mm



PIN CONNECTIONS



BLOCK DIAGRAM



TRUTH TABLE (positive logic)

INPUTS (M 1025 output code)						OUTPUTS													
E	A	B	C	D	G	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
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1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	1	1	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	0	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
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1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
X	X	X	X	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	17 to 19	V
V_I	Input voltage	0 to V_{DD}	V
$V_{O\,(off)}$	Off state output voltage (M055 type)	19	V
T_{op}	Operating temperature	0 to 70	°C

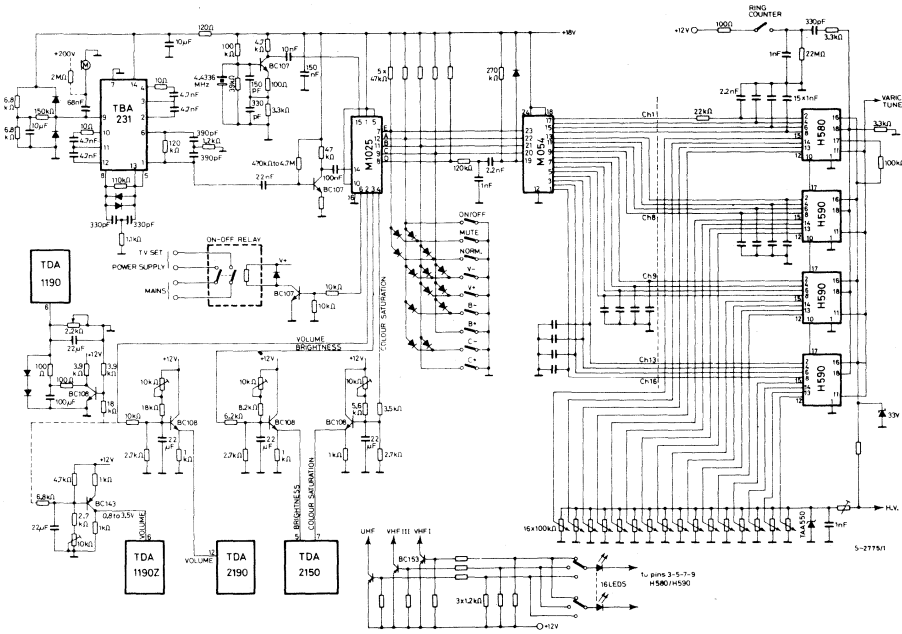
STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions		Values at 25°C			Unit
					Min.	Typ.	Max.	
V_{IH}	High level input voltage	A-B-C-D-E Inputs			V_{DD}-1		V_{DD}	V
		G Input			3		V_{DD}	
V_{IL}	Low level input voltage	A-B-C-D-E Inputs			0		V_{DD}-4	V
		G Input			0		0.3	
I_{OL}	Low level output current		V_{DD}= 17V	V_{OL}= 0.4V	1.6			mA
I_{OH}	High level output current (M 055 Type)		M 054 Type	V_{DD}= 19V V_{OH}= 8V			-200	µA
$I_{O(off)}$	Off state output current (M 054 Type)		M 055 Type V_{DD}= 19V	$V_{O(off)}$= 8V			1	µA
I_{DD}	Supply current		V_{DD}= 19V All input to V_{SS}				25	mA

TYPICAL APPLICATIONS

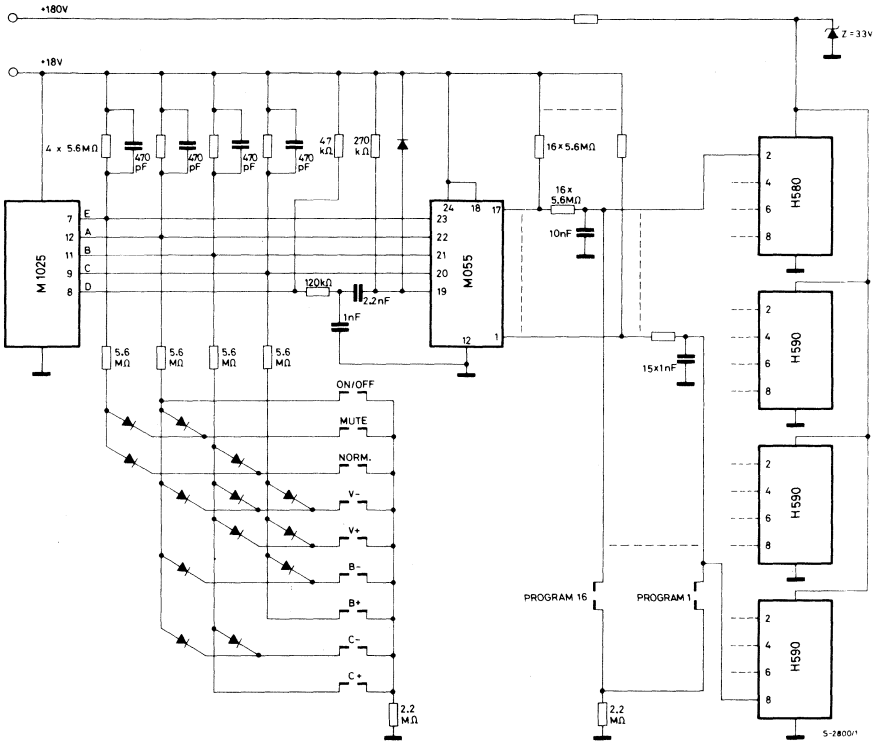
Fig. 1 and 2 show a typical application of M 054 and M 055 respectively in a TV remote control system.

Fig. 1 - M054 with light pressure switches



TYPICAL APPLICATIONS (continued)

Fig. 2 - M055 with direct touch controls



MOS INTEGRATED CIRCUITS

M 082/A
M 083/A
M 086/A

PRELIMINARY DATA

TONE GENERATOR

- SINGLE POWER SUPPLY
- WIDE SUPPLY VOLTAGE OPERATING RANGE
- LOW POWER DISSIPATION < 500 mW
- 13 (M082/A, M083/A) OR 12 (M086/A) TONE OUTPUTS
- HIGH OUTPUT DRIVE CAPABILITY
- HIGH ACCURACY OF OUTPUT FREQUENCIES: ERROR LESS THAN ± 0.069%
- INPUT PROTECTED AGAINST STATIC CHARGES
- LOW INTERMODULATION

The M082/A, M083/A and M086/A are monolithic tone generators specifically designed for electronic organs. The only difference between the M082, M083, M086 and the M082A, M083A, M086A is the maximum input clock frequency, which is 4500 KHz for the standard types and 2500 KHz for the "A" types. Constructed on a single chip using low threshold N-channel silicon gate technology they are supplied in a 16 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

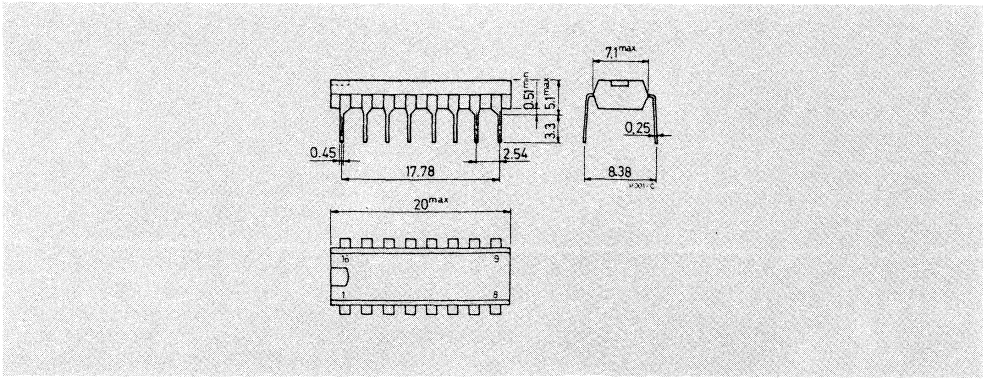
V_i	Voltage on any pin relative to V_{SS} (GND)	+20 to -0.3	V
T_{op}	Operating temperature	0 to 50	°C
T_{stg}	Storage temperature	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

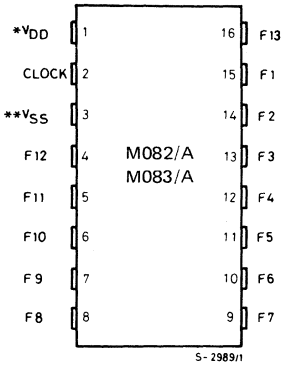
ORDERING NUMBERS: M082B1 M082A B1
M083B1 M083A B1
M086B1 M086A B1

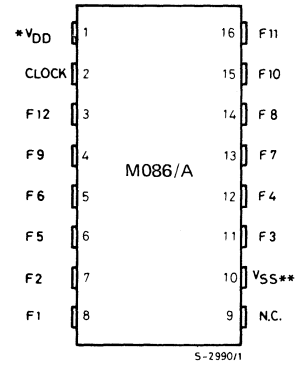
MECHANICAL DATA

Dimensions in mm



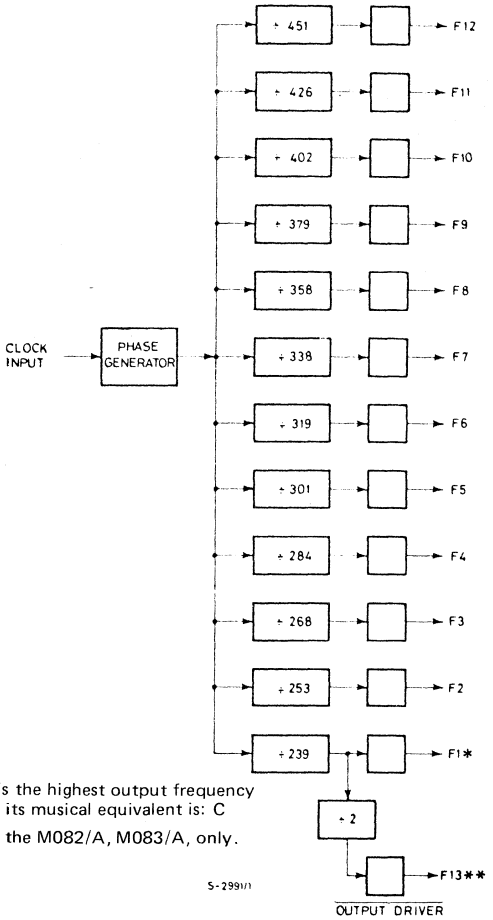
PIN CONNECTIONS





* V_{DD} is the highest supply voltage
** V_{SS} is the lowest supply voltage

BLOCK DIAGRAM



* F1 is the highest output frequency and its musical equivalent is: C
** For the M082/A, M083/A, only.

RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{SS}	Lowest supply voltage		0		0	V
V_{DD}	Highest supply voltage		+10	+12	+14	V

ELECTRICAL CHARACTERISTICS ($0°C \leq T_{amb} \leq 50°C$; $V_{SS}=0V$; $V_{DD}=+10V$ to $+14V$ unless otherwise specified)

Parameter		Test conditions	Values			Unit	Fig.
			Min.	Typ.	Max.		
V_{IL}	Input clock, low		V_{SS}		$V_{SS}+1$	V	1
V_{IH}	Input clock, high		$V_{DD}-1$		V_{DD}	V	
t_r, t_f	Input clock rise and fall times 10% to 90%	4.5 MHz			30	ns	1
t_{on}, t_{off}	Input clock on and off times	4.5 MHz		111		ns	1
C_I	Input capacitance			5	10	pF	
V_{OH}	Output high	0.75 mA	$V_{DD}-1.5$		V_{DD}	V	2
V_{OL}	Output low	0.70 mA	V_{SS}		$V_{SS}+1$	V	2
t_{ro}, t_{fo}	Output rise and fall times 500 pF load		250		2500	ns	3
t_{on}, t_{off}	Output duty cycle	M 082		30		%	
		M 083, M 086		50			
I_{DD}	Supply current			24	35	mA	*
f_I	Input clock frequency	M082, M083, M086	100	4000.48	4500	kHz	
f_I	Input clock frequency	M082A, M083A, M086A	100	2000.24	2500	kHz	

* Output unloaded.

Fig. 1 Input clock waveform

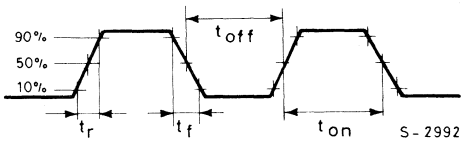


Fig. 2 - Output signal d.c. loading

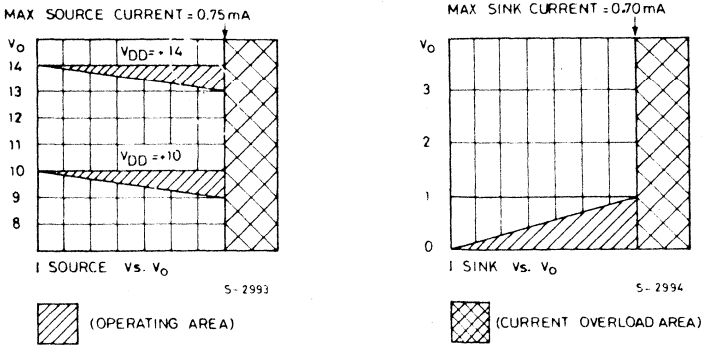
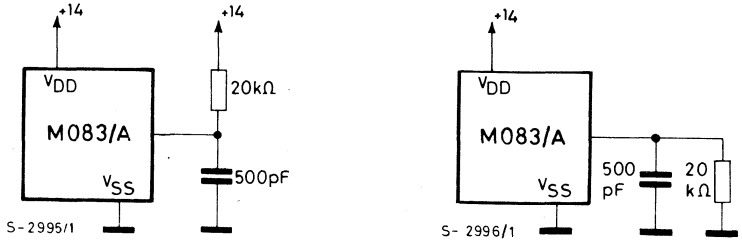


Fig. 3 - Output loading



2 x 8 CROSSPOINT MATRIX

- VERY LOW ON RESISTANCE
- HIGH CROSS-TALK AND OFF-STATE ISOLATION
- SERIAL SWITCH ADDRESSING, μ-PROCESSOR COMPATIBLE

The M089 and M099 are 2x8 crosspoint matrices consisting of 16 N-channel MOS transistors. Both devices are similar in operation, the only difference being that in the M099 the "all switches reset" function is implemented by a microprocessor command.
Both devices have been specially designed to provide switches with low cross-talk, high off-state isolation (both better than -90 dB) and low on-resistance.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.5 to 17	V
V_I	Input voltage pins 4, 5, 12, 13	-0.5 to 17	V
V_{IN}-V_{OUT}	Differential voltage across any disconnected switch	10	V
P_{tot}	Total power dissipation	640	mW
T_{op}	Operating temperature range: for plastic	0 to 70	°C
	for ceramic	-40 to 70	°C
T_{stg}	Storage temperature range	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

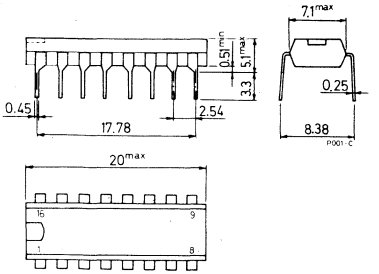
** With respect to V_{SS} (GND) pin.

ORDERING NUMBERS:

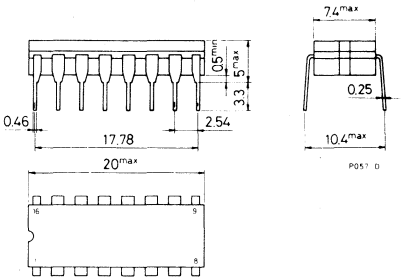
M089/M099 B1 for dual-in-line plastic package
M089/M099 D1 for dual-in-line ceramic package
M089/M099 F1 for dual-in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

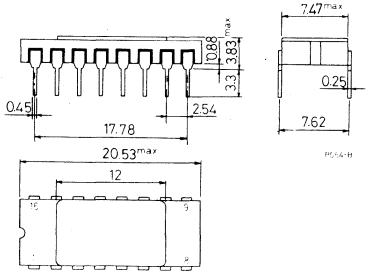
Dual-in-line plastic package



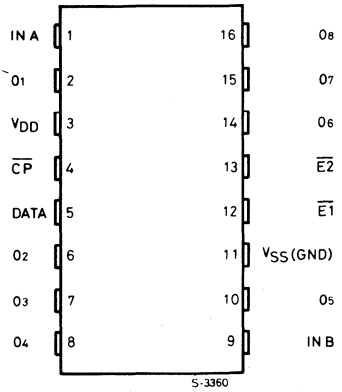
Dual-in-line ceramic package frit seal



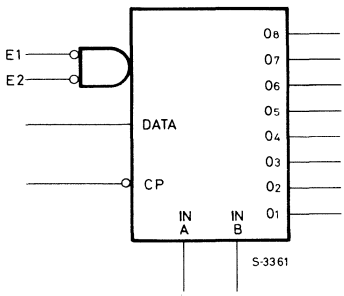
Dual-in-line ceramic package



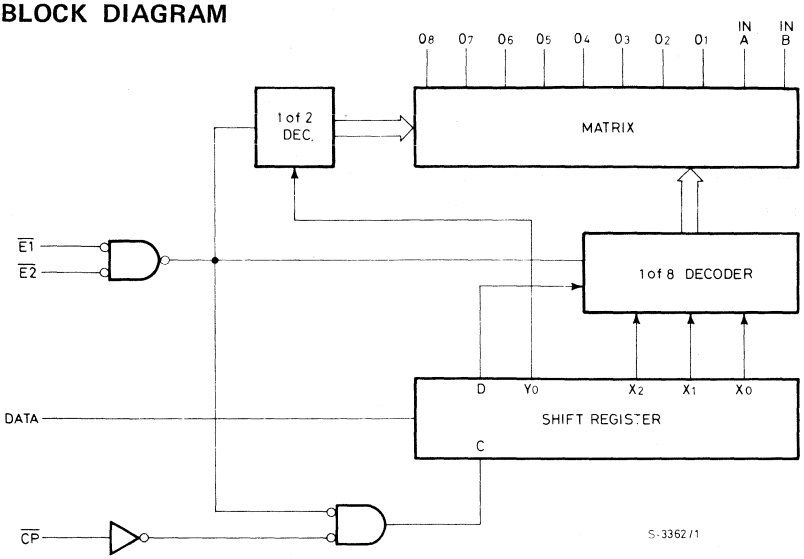
PIN CONNECTIONS



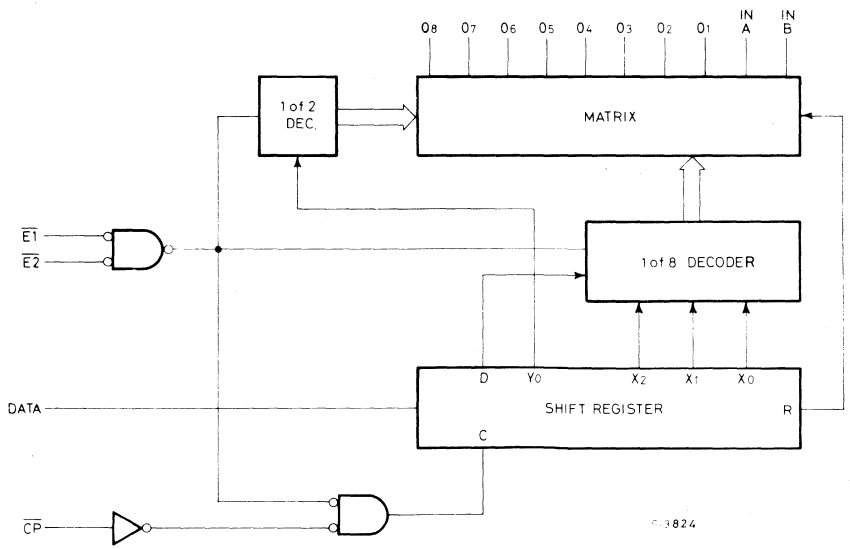
LOGIC DIAGRAM



M089 BLOCK DIAGRAM



M099 BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The M089 and M099 are capable of forming any combination of switch conditions in an 8x2 matrix. Each switch is individually set and a latch maintains it in its set condition.
The switch address and control bits are loaded serially into an internal shift register (5 bit for M089, 6 bit for M099) when inputs E_1, and E_2 are low. The address bits in both matrices consist of: 3 input selection bits (X_0-X_2) and a single output selection bit (Y_0). A fifth (control) bit (D) defines whether the chosen switch is to be opened or closed.
In the M099 a sixth bit (R) is an "all switch reset". Reset occurs on the low to high transition of the enable inputs when both D and R are zero.
During normal selection the R bit must be a 1.

D	Y_0	X_2	X_1	X_6

M089 Shift Register Bit Allocation

D	Y_0	X_2	X_1	X_0	R

M099 Shift Register Bit Allocation

0	X	X	X	X	0

M099 Reset Word.

Data bits are clocked into the shift register on the high to low transition of the clock input (CP). If more than 5 (or 6 in the case of the M090) clock transmission are applied during loading of the shift register the last 5 (or 6) data bits are loaded into it. The status of the switch addressed changes on the low to high transition of one or both enable inputs.

ENABLE INPUTS TRUTH TABLE

$\overline{E}_1$	$\overline{E}_2$	FUNCTION M089	FUNCTION M099
L	L	Data Load	
⌐	L	addressed switch changed	addressed switch changed or all switch reset
L	⌐		
⌐	⌐		

DATA BIT TRUTH TABLE

– M089 –	
Data	**Switch status after enable transition**
L	disconnect
H	connect

DATA AND RESET BIT TRUTH TABLE

– M099 only –		
D	**R**	**Switch status**
L	L	all switches reset
H	L	no change
L	H	addressed switch disconnected
H	H	addressed switch connected

DATA BITS TRUTH TABLE FOR SWITCH SELECTION

	O_1 Y_0 X_2 X_1 X_0	O_2	O_3	O_4	O_5	O_6	O_7	O_8
IN A	1111	1011	1101	1001	1110	1010	1100	1000
IN B	0111	0011	0101	0001	0110	0010	0100	0000

For example to address the switch connecting IN A to O_5 the shift register must be loaded with the code:

	M089	**M099**
	D Y_0 X_2 X_1 X_0	**D Y_0 X_2 X_1 X_0 R**
to connect	11110	111101
to disconnect	01110	011101

ELECTRICAL CHARACTERISTICS (T_{amb}= 0 to 70°C for M089/M099 B1; -40 to 70°C for M089/M099 F1, D1; V_{DD}= 14V to 16V unless otherwise specified)

Parameter			Test conditions	Min.	Typ.	Max.	Unit
R_{ON}*	ON-resistance		T_{amb}= 25°C $V_{i\ (A,\ B)}$= 3.5V V_{DD}= 14V $I_{D(min)}$= 10 mA		10	15	Ω
ΔR_{ON}	ON-resistance variation in any package		T_{amb}= 25°C V_i= 3.5V V_{DD}= 14V I_D= 10 mA			± 2	%
I_{DD}	Supply current					7	mA
I_{LI}	Input leakage	pins 4, 5 12, 13	V_i= 5V			1	μA
		pins 1, 9	V_{iA}, V_{iB}= 4.5V V_{O1}, V_{O8}= 1.5V			0.2	μA
			V_{iA}, V_{iB}= 6V V_{O1}, V_{O8}= 1.5V			1	μA
I_{LO}	Output leakage	pins 2, 6, 7 8, 10, 14 15, 16	V_{O1}, V_{O8}= 4.5V V_{iA}, V_{iB}= 1.5V			0.2	μA
			V_{O1}, V_{O8}= 6V V_{iA}, V_{iB}= 1.5V			1	μA
V_{low}	Logic 0 input level		All inputs	-0.3		0.8	V
V_{high}	Logic 1 input level		All inputs	4.5		V_{DD}	V
CT	Cross-talk attenuation		See fig. 4	90	95		dB
I_O	Off isolation		See fig. 5	90	95		dB
f_{CL}	Maximum clock input frequency		See fig. 6 for M089 See fig. 7 for M099			1	MHz
T_{LG}	Lag time			100			ns
T_{LD1}	Lead time			400			ns
T_{LD2}				150			
T_{WR}	Write time					3	μs
t_W	Clock pulse width			0.4		100	μs

* See fig. 1 and 2 for R_{ON} variation with temperature and V_{BIAS}.

Fig. 1 - R_{ON} derating vs. temperature typ.

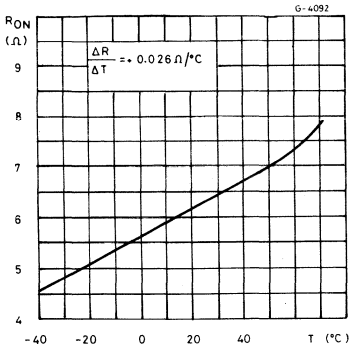
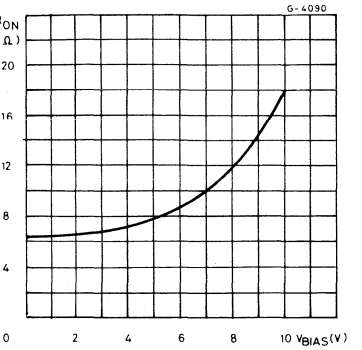


Fig. 2 - R_{ON} derating vs. V_{BIAS}.



TEST CIRCUITS

Fig. 3 - R_{ON} measurement

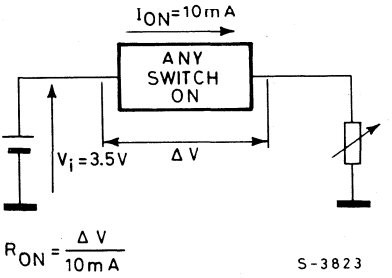


Fig. 4 - Crosstalk measurements

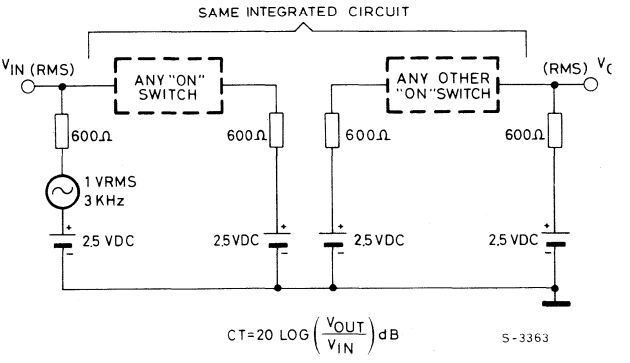
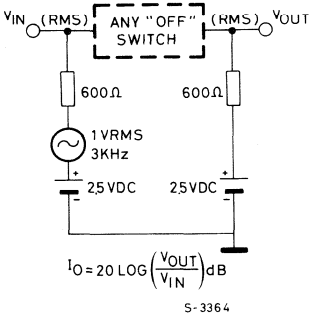


Fig. 5 - Off isolation measurement



TIMING DIAGRAMS

Fig. 6 - M089 timing diagram

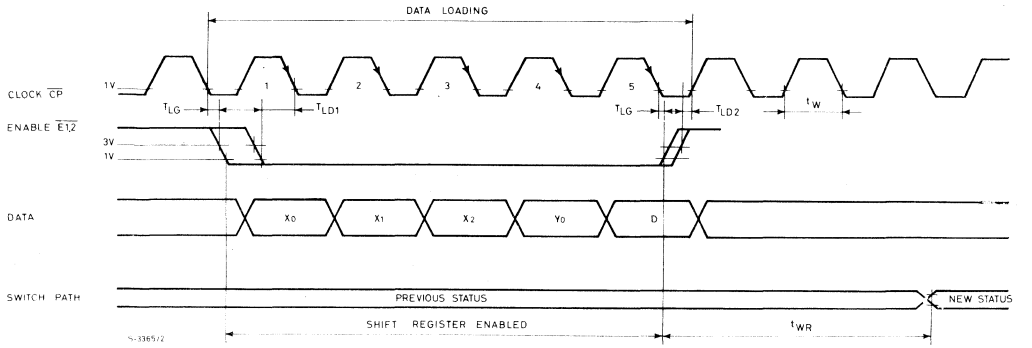
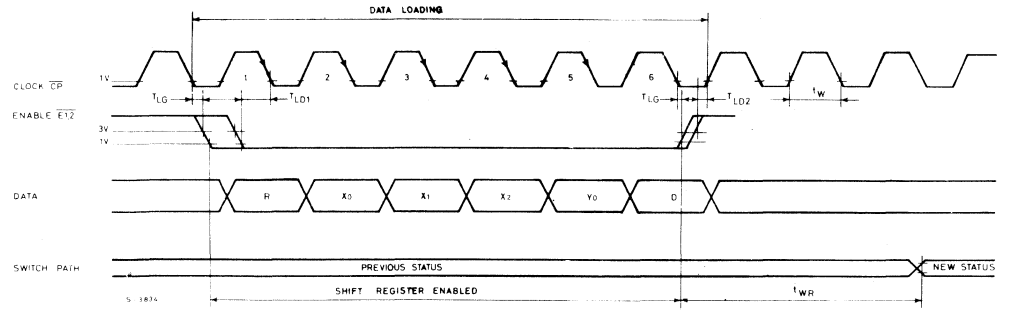


Fig. 7 - M099 timing diagram



MOS INTEGRATED CIRCUIT

M 090

ADVANCE DATA

A - LAW SINGLE CHANNEL PCM CODEC

- ± 5V SUPPLY
- FOLLOWS CCITT A-LAW COMPANDING CODE
- EXCEEDS CCITT SPECIFICATIONS
- INDEPENDENT RECEIVE AND TRANSMIT SECTIONS
- FULLY ASYNCHRONOUS
- ON-CHIP AUTOZERO
- LOW EXTERNAL COMPONENT COUNT
- SEPARATE ANALOG AND DIGITAL GROUNDS
- SINGLE 16-PIN PACKAGE
- TTL COMPATIBLE

The M090 is a monolithic N-channel silicon-gate PCM CODEC (coder-decoder) which performs analog-to-digital conversion (coding) and digital-to-analog conversion (decoding) using the A-Law companding code. It is intended for use as a per-channel voice frequency CODEC in telephone systems but features completely independent ADC and DAC sections to permit asynchronous transmission/reception. Transmission and reception is in form of 8 bit words at a data rate up to 2.048M bits/sec using audio sampling at 8 KHz. Capacitive network AD and DA converters are used to ensure high long term stability and immunity to temperature variations. The maximum power consumption is 90 mW (70 mW typ). The M090 is available in a 16-lead dual in-line plastic and ceramic package.

ABSOLUTE MAXIMUM RATINGS*

$V+$**	Positive supply voltage	+7.5	V
$V-$	Negative supply voltage	-7.5	V
V_{DI}	Digital inputs	-0.3 to 10	V
V_{AI}	Analog inputs	$V- \leqslant V_I \leqslant V+$	V
$+V_{ref}$	Positive reference voltage	$-0.3 \leqslant V_I \leqslant V+$	V
$-V_{ref}$	Negative reference voltage	$V- \leqslant V_I \leqslant 0.3$	V
P_{tot}	Power dissipation	400	mW
T_{op}	Operating temperature range	0 to 70	°C
T_{stg}	Storage temperature range	-55 to 125	°C

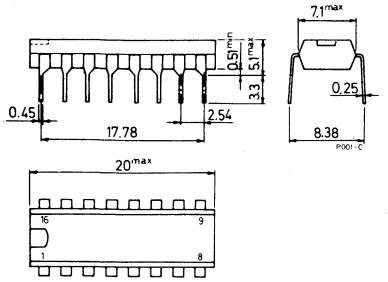
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** With respect to Analog or Digital ground.

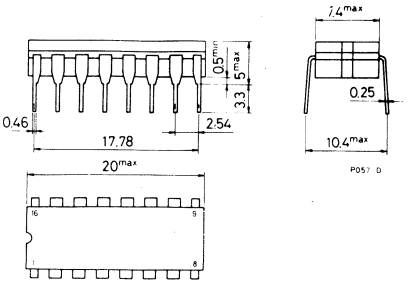
ORDERING NUMBERS: M090 B1 for dual-in-line plastic package
M090 F1 for dual-in-line ceramic package (frit seal)

MECHANICAL DATA (dimensions in mm)

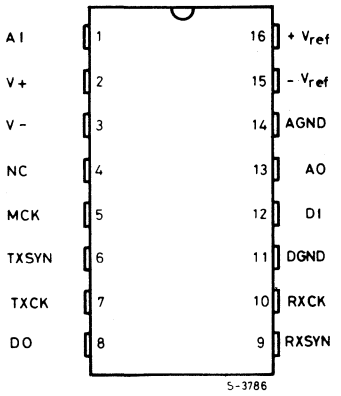
Dual in-line plastic package



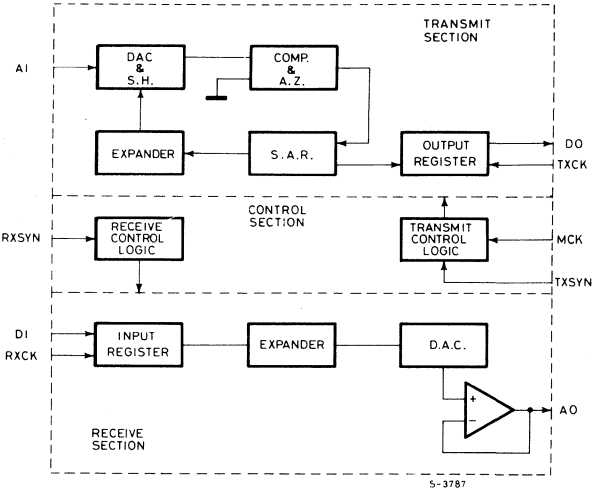
Dual in-line ceramic package, frit seal



PIN CONNECTIONS



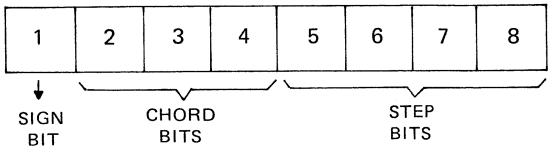
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Data word format

The eight bit words used for transmission and reception consist of a sign bit and seven magnitude bits. The magnitude bits are further divided into three chord bits and four step bits. The sign bit, which indicates the polarity of the analog signal, is the first to be transmitted and is thus the first to be received. The division of the seven magnitude into chord and step bits is to obtain higher ADC resolution at low (analog) signal levels. The analog value of each step bit is doubled for each successive chord, i.e. for the first two chords the step bit value is 1.2 mV; for the third chord the step value is 2.4 mV; for the fourth, 4.8 mV etc.



Analog Input (AI), pin 1

The audio signal supplied to this input is sampled at 8 kHz and coded. The input level on this pin must always be between $+V_{ref}$ and $-V_{ref}$.

Master Clock (MCK), pin 5

The Master Clock is used to time conversion operations and is completely independent of the transmit and receive clocks (TXCK and RXCK).

Transmit Sync (TXSYN), pin 6

This input enables the transmission output register. The TXSYN signal is synchronised to the transmit clock and lasts eight TXCK periods.

Transmit Clock (TXCK), pin 7

This determines the transmission rate and may be up to 2.1 MHz.
Each of the eight bits in the output register is transmitted when the logic AND of TXSYN and TXCK is true.

Digital Output (DO), pin 8

The eight bit word stored in the transmission register is shifted out via the Digital Output by TXCK when TXSYNC is high. When TXSYNC is low this output is in the high impedance condition.,
The M090 also provides inversion of the even bits (bits 2, 4, 6, 8).

Receive Sync (RXSYN), pin 9

This input is synchronised with the receive clock and lasts eight RXCK periods, enabling the PCM input to the receive register.

Receive Clock (RXCK), pin 10

Each of the 8 bits of the input word is loaded by the receive clock when RXSYNC is high. RXCK may be completely asynchronous with the transmit clock.

FUNCTIONAL DESCRIPTION (continued)

Digital Input (DI), pin 12

The eight bit receive register is loaded via the Digital Input.

Analog Ground and Digital Ground (AGND, DGND), pins 14, 11

Separate grounding pins are provided for the digital and analog parts of the circuit to prevent signal degradation. The same criteria should be applied during the design of the P.C. board on which CODEC and filters are mounted.

Analog Output (AO), pin 13

The PCM word loaded into the input register is transferred to the DAC for conversion to the analog signal. This signal, in the form of 100% duty cycle voltage steps, reaches the Analog Output via a low impedance buffer. A low-pass filter must be connected to this output to recreate the voice signal.

Reference Voltages ($+V_{ref}$, $-V_{ref}$), pins 16, 15

The D/A converter reference voltages are connected to these pins. The difference between the absolute values of $+V_{ref}$ and $-V_{ref}$ must be less than 1%.

ELECTRICAL CHARACTERISTICS (All parameters are tested at $T_{amb}=25°C$, $V^+=5V$, $V^-=5V$)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Note
STATIC ELECTRICAL CHARACTERISTICS							
V^+	Positive supply voltage		4.75	5.0	5.25	V	
V^-	Negative supply voltage		-5.25	-5.0	-4.75	V	
$+V_{ref}$	Positive reference voltage		2.375	2.5	2.625	V	
$-V_{ref}$	Negative reference voltage		-2.625	-2.5	-2.375	V	
R_{IS}	AI resist. during sampling			200		Ω	
R_{INS}	AI resistance non sampling			10		MΩ	
R_O	AO resistance			50		Ω	
V_{OH}	Digital output	I_{OH}= 5 mA	4.5			V	
V_{OL}	Digital output	I_{OL}= 5 mA			0.5	V	
V_{IH}	Pins 5, 6, 7, 9, 10		2			V	
V_{IL}	Pins 5. 6. 7. 9. 10				0.8	V	
I^+	Positive supply current			9	11	mA	
I^-	Negative supply current			5	7	mA	

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Note
DYNAMIC ELECTRICAL CHARACTERISTICS (see Fig. 1)							
t_{WS}	TXSYN, RXSYN width			8/FX(FR)		μs	
t_{XCS}	TXCK to TXSYN delay		25		1/FX-80	ns	1
t_{SDON}	DO to TSYN on delay				90	ns	2
t_{SDOFF}	DO to TXSYN off delay				70	ns	2
t_{CDXH}	DO high to TXCK delay				200	ns	2
t_{CDXL}	DO low to TXCK delay				180	ns	2
t_{DOR}	DO rise time			40		ns	2
t_{DOF}	DO fall time			20		ns	2
t_{SRC}	RSYN to RXCK delay		50		1/FR-50	ns	1
t_{CDRS}	DI to RXCK set up time		10			ns	
t_{CDRH}	DI to RXCK hold time		60			ns	
t_{SAO}	AO to RXSYN delay	for sample n - 1		800		ns	
t_{RC}	Clock rise time				50	ns	
t_{FC}	Clock fall time				50	ns	
M_{CKF}	MCK frequency				2.1	MHz	
FX, FR	TXCK, RXCK, frequency		0.064		2.1	MHz	
CK D.C.	TXCK, RXCK duty cycle		40	50	60	%	
$SLEW^+$	AO positive slew rate				5	V/μs	
$SLEW^-$	AO negative slew rate				5	V/μs	
SYSTEM CHARACTERISTICS (see Fig. 2 and 3)							
S/Q	Total distortion	AI = -1 dBm 0		30		dB	3
		AI = -15 dBm 0		38		dB	3
		AI = -34 dBm 0		35		dB	
		AI = -50 dBm 0		20		dB	3
ΔG/G	Gain traking	AI = +3 dBm 0		0		dB	4
		AI = -20 dBm 0		0		dB	4
		AI = -50 dBm 0		±0.15		dB	4
		AI = -55 dBm 0		±0.2		dB	4
	Idle channel noise			-80	-74	dBmOp	

Note: 1) FR and FX are expressed in Hz.
2) Driving one 74 LS TTL load plus 30 pF.
3) The signal at the analog input is a pseudorandom noise (350 ÷ 550 Hz).
4) The signal at analog input is a 840 Hz sinewave.

Fig. 1 - Transmit and receive sections

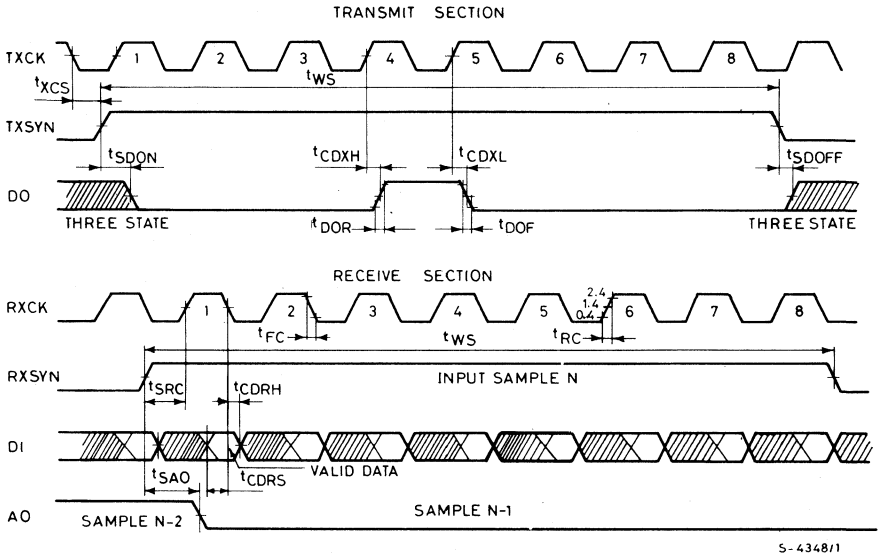


Fig. 2 - S/Q ratio vs. input level.

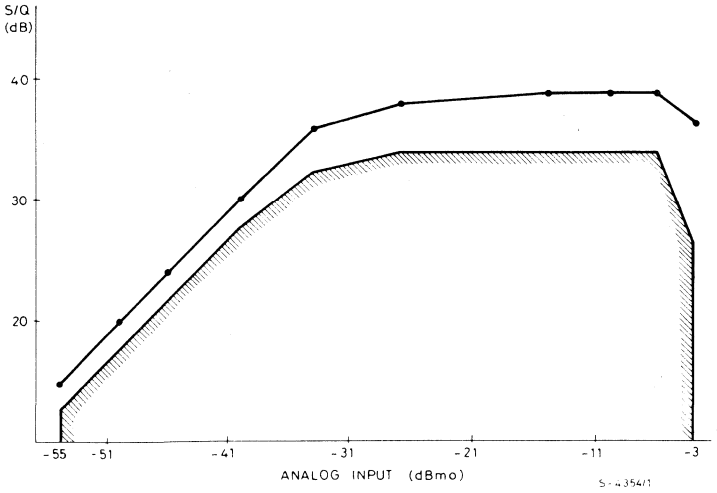
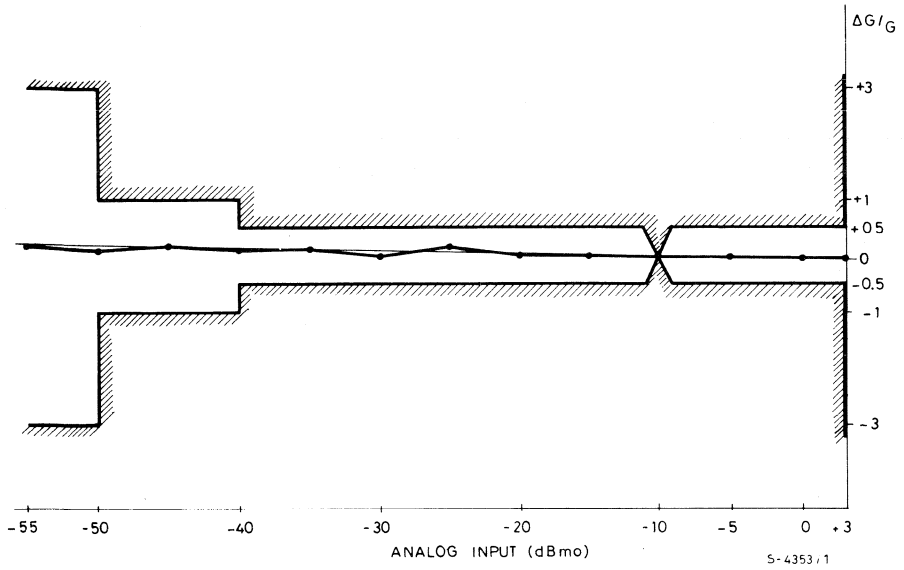


Fig. 3 - Gain tracking performance



ON-SCREEN TUNING SCALE AND BAND DISPLAY

- DIGITAL TUNING BAR DISPLAY WITH MINIMUM EXTERNAL PRESETS
- ON-SCREEN DISPLAY OF THE BAND
- VERTICAL POSITION ON THE SCREEN EXTERNALLY ADJUSTABLE
- AUTOMATIC DISPLAY AT SEARCH COMMAND
- DESIGNED FOR USE WITH THE M193 ELECTRONIC PROGRAM MEMORY
- M191: STANDARD VERSION
- M091: FOR AUTOMATIC SEARCH IN FRENCH STANDARD APPLICATIONS

The M091 and M191 are monolithic integrated circuits designed to display on the screen of the television receiver a variable length strip corresponding to the voltage applied to the varicap tuner.
A variable number of rectangles symbolizing the selected band can also be displayed.
The circuits operate in conjunction with the M193 (Electronic Program Memory), from which they take the voltage and band information in a digital serial mode.
The 7 most significant digits of voltage information coming from the M193 are digitally converted into a 64 step variable pulse width giving either positive and negative polarity outputs for easy and versatile interfacing.
The variable length strip is displayed over 11 lines of a half frame picture with nine vertical graduations of 31 lines.
The vertical position of the strip can be adjusted with an external potentiometer over the whole screen.
The 2 digits of band information determine the number of rectangles appearing on the screen under the tuning strip. The rectangles are displayed over 11 lines of a half frame picture.
Automatic display is provided when the Electronic Program Memory is in the Search Mode; display on manual command is also possible.
The M191 is the standard version. The M091 is alternatively for displaying the tuning voltage when the automatic search is made by scanning the band in a reverse way (i.e. from 30 to 0V) as is required by the French standard.
The M091 displays 30V (maximum length of the strip) when the M193 Electronic Program Memory transmits information corresponding to 0V. It displays 0V when the M193 transmits information corresponding to 30V.
It displays 0V when the M193 transmits information corresponding to 30V.
The M091 and M191 are constructed in N-channel silicon gate technology and are available in a 16 pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

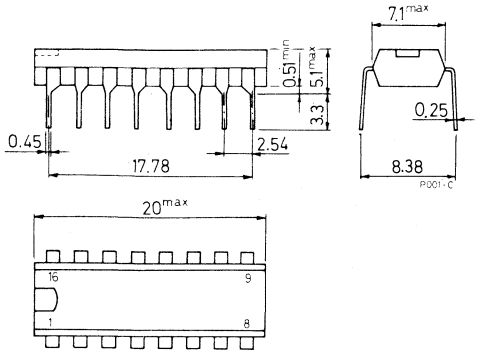
V_{DD} **	Supply voltage	-0.3 to 20	V
V_I	Input voltage	-0.3 to 20	V
I_I	Input current	-5	mA
$V_{O\,(off)}$	Off-state output voltage	20	V
I_O	Output current (except pins 12-13)	5	mA
	(pins 12-13)	15	mA
P_{tot}	Total package power dissipation	500	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

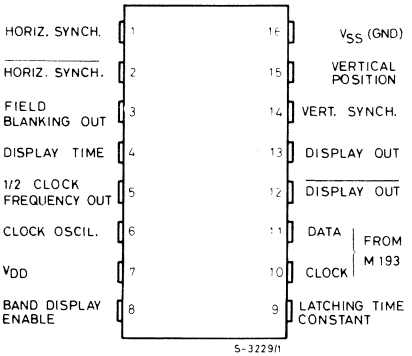
** All voltages are with respect to V_{SS} (GND).

ORDERING NUMBERS: M191 B1
M091 B1

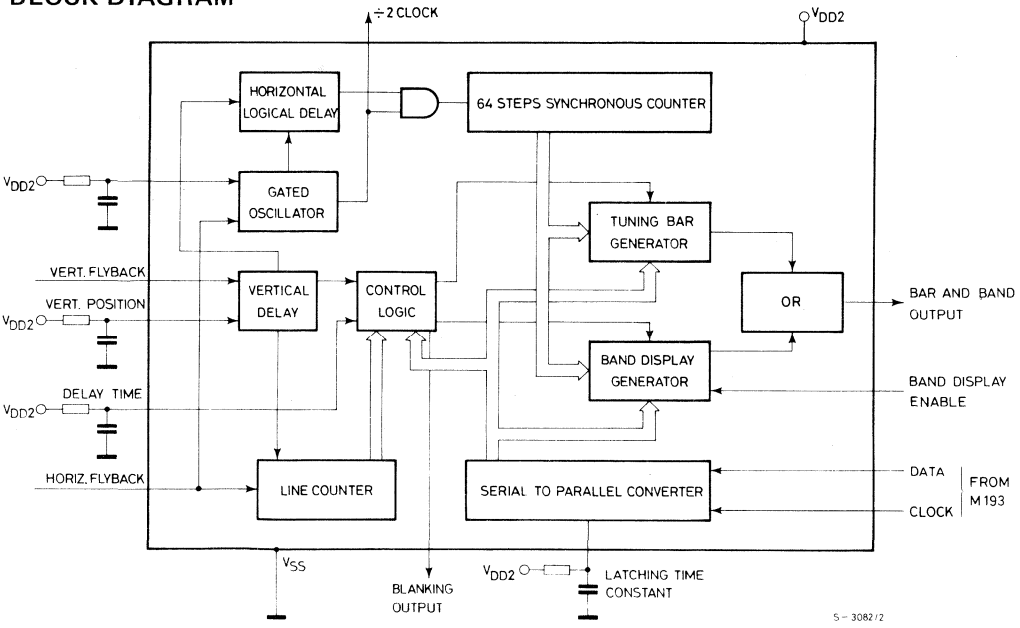
MECHANICAL DATA (dimensions in mm)



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	Parameter	Min.	Typ.	Max.	
V_{DD}	Supply voltage	11.5	13	14.5	V
V_I	Input voltage			14.5	V
$V_{O\,(off)}$	Off-state output voltage			14.5	V
I_O	Output current - all pins except 4-6-12-13*			1	mA
	- pin 6			3	mA
	- pins 12-13			10	mA
f	Clock frequency		1.8	2.2	MHz
T_{op}	Operating temperature	0		70	°C
P_{tot}	Total package power dissipation			500	mW
C_9	Capacitance at pin 9		330	390	pF
C_6	Capacitance at pin 6		68	100	pF
C_{15}	Capacitance at pin 15		270	330	nF
C_4	Capacitance at pin 4**		10	12	μF
$R_{4,\,15}$	Resistance at pins 4-15		220	270	KΩ

* I_{O4} The output current of pin 4 is internally limited.
** C_4 Values up to 100 μF are allowed using a 1KΩ resistor in series with pin 4.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions).

Typical values are at T_{amb}= 25°C, V_{DD}= 13V.

Parameter		Test conditions	Pins	Values			Unit
				Min.	Typ.	Max.	
V_{IL}	Low level input voltage	V_{DD}= 11.5 to 14.5V	1-2-10-11-14			0.8	V
V_{IH}	High level input voltage	V_{DD}= 11.5 to 14.5V	1-2-10-11-14	3.5			V
V_{OL}	Low level output voltage	V_{DD}= 11.5V I_{OL} = 10 mA	12-13			1	V
		V_{DD}= 11.5V I_{OL}= 1 mA	3			1	V
V_T	Threshold voltage	V_{DD}= 11.5 to 14.5V	6-9-15		4		V
			4-8		2		
I_I	Input current	V_I = 14.5V				10	μA
$I_{O\,(off)}$	Off-state output current	V_{DD} = 14.5V	3-4-5-9-15			20	μA
			12-13			100	
I_{DD}	Supply current	V_{DD}= 14.5V				25	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C)

Parameter	Test conditions	Values			Unit
		Min.	Typ.	Max.	
t_{TLH}, t_{THL} Transition time	Pins 12-13 See fig. 3		80		ns
t_D Delay time			50		ns

TYPICAL APPLICATION

Fig. 1

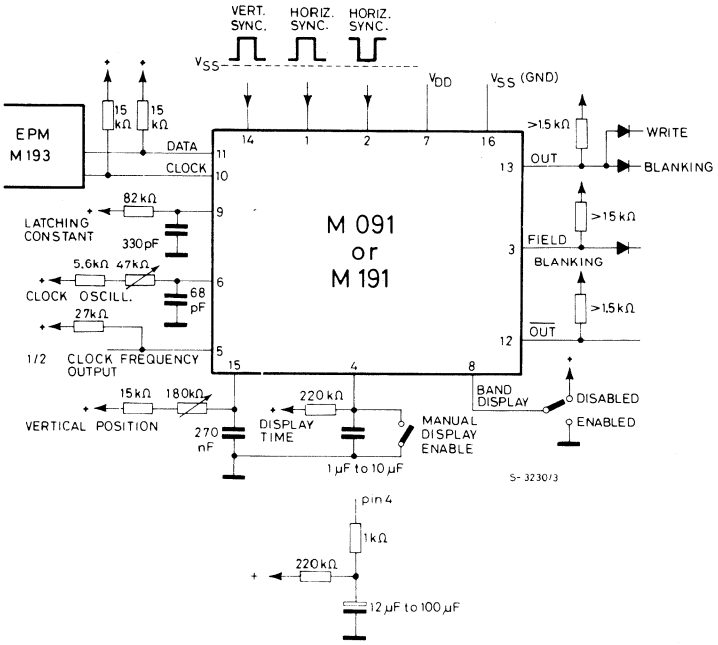
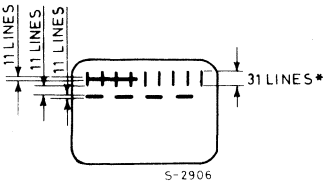
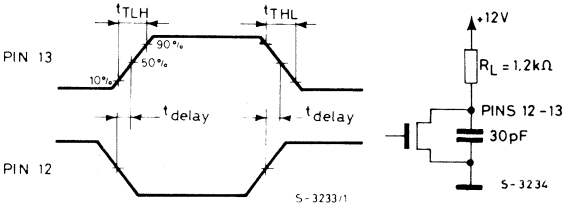


Fig. 2



* : THE LINES CORRESPOND TO A HALF FRAME

Fig. 3

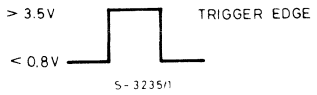


DESCRIPTION

Pins 1, 2 - Horizontal synchronization

Two Horizontal sync inputs are provided to allow for positive or negative pulses from the TV receiver. Pin 1 is designed to accept a positive pulse derived from the line flyback through an interface.
The circuit is triggered on the negative edge of the incoming pulse.

Fig. 4 - Pin 1



The negative flyback pulses must be applied to pin 2. In this case the circuit is triggered on the positive edge of the pulse.

Fig. 5 - Pin 2

The display is delayed for a time corresponding to 32 clock periods after the triggering.
With a clock frequency of 1.8 MHz the delay is 9 μsec.
When pin 1 is used, pin 2 must be connected to V_{SS} (GND); when using pin 2, pin 1 must be at V_{DD}.

Pin 3 - Field blanking output

An open drain transistor is disabled during the lines which correspond to the display of the tuning scale and band information. This makes it possible to write the tuning scale and the band identification rectangles on a dark or alternative colour area. The signal is present for the full line period.

Pin 4 - Display time input

The display is automatically enabled when the M193 (Electronic Program Memory) is in the Search mode.
The RC network applied to pin 4 determines the time the display will last after a station is found.
When identification occurs the capacitor is unclamped and allowed to be charged by the external resistor.
The display is disabled when an internal threshold is reached.
The display is also enabled if the capacitor is discharged by connecting this pin to V_{SS} (GND) with an external clamp.
If a capacitor $>$ 10 μF is used a 1 KΩ resistor must be placed in series with pin 4.

Pin 5 - 1/2 frequency clock output

The clock frequency divided by two is present on this pin for measurement purposes. To allow this, connect temporarily pin 1 to V_{SS} and pin 2 to V_{DD}. The output is open drain and an external pull-up resistor is needed.
If the output is not used it must be connected to V_{SS}.

DESCRIPTION (continued)

Pin 6 - Clock oscillator input

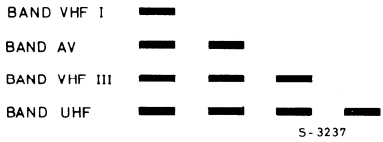
This pin is connected to a RC network as shown in fig. 1.
The clock frequency determines the horizontal width on the screen of the tuning scale, of the rectangles and the distance of the display from the left edge of the screen.
Fine adjustment of the clock frequency is obtained by the trimming resistor. Typical clock frequency is 1.8 MHz.

Pin 7 - V_{DD}

Pin 8 - Band display enable

When this pin is connected to V_{SS} (GND) a band display with the following format is enabled, on command, together with the tuning voltage display.

Fig. 6

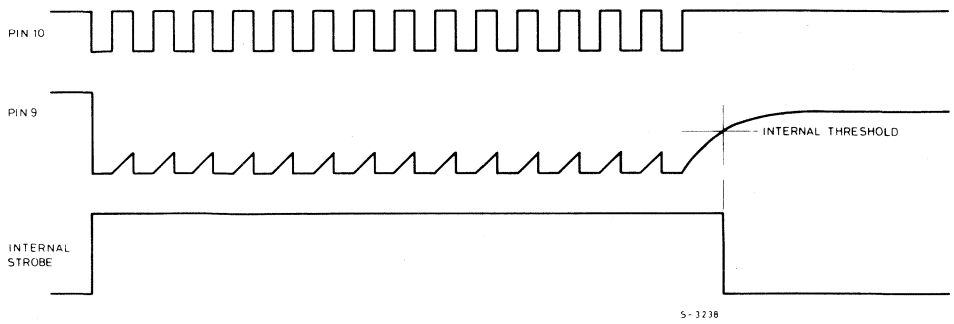


If this pin is connected to V_{DD} only the tuning voltage will be displayed.

Pin 9 - Latching time constant

An RC time constant must be applied to this pin to generate the internal latching signal.
The content of the internal shift register is transferred to the internal decoding circuit only at the end of the clock burst to avoid noise on the display during data transfer.
This is made by integrating the incoming clock burst with the RC time constant connected to pin 9 as shown in fig. 7.

Fig. 7

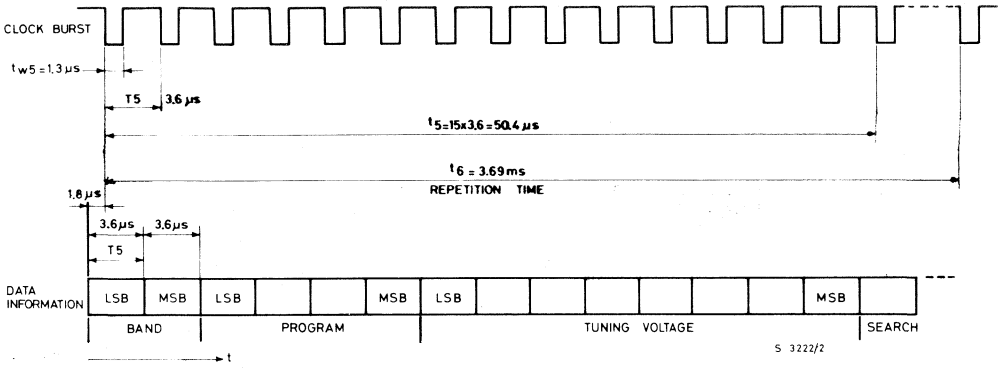


DESCRIPTION (continued)

Pin 10 - Clock input

This pin accepts the burst containing the 15 clock pulses available from the M193. The burst is used to load the serial Data on pin 11 into the internal 15 bit shift register (see fig. 8).

Fig. 8



Pin 11 - Data input

This pin accepts the 15 bit serial Data information available from the M193 EPM.
The burst contains 2 bits for band information, 4 bits for program, 8 bits for tuning voltage and 1 bit which indicates if the system is in the Search mode.

Pin 12 - Inverted video signal output

The signals of pin 13 are inverted and presented on this pin to allow easy interfacing in some chroma kits. The output is open drain.

Pin 13 - Video signal output

The tuning scale and band information video signal is available on this pin, a load resistor is connected between the open drain output transistor and V_{DD}. White level corresponds to disable of the internal transistor.

Pin 14 - Vertical synchronization

The frame flyback pulse must be applied to this pin by means of an interface. The signal must be positive. The circuit is triggered by the negative edge of the pulse.

Fig. 9

DESCRIPTION (continued)

Pin 15 - Vertical position input

An internal monostable is triggered by the frame pulse applied on pin 14.
The display is allowed at the end of the cycle of the monostable. The RC network applied to this pin gives the time constant of the monostable determining the position of the display on the screen.

Pin 16 - V_{SS} (GND)

All voltages quoted are referred to Pin 16.

MOS INTEGRATED CIRCUIT

M 106

TV MICROPROCESSOR INTERFACE

- 6 PWM D/A CONVERTERS, WITH 64 STEP RESOLUTION, FOR ANALOGUE CONTROLS
- 13 BIT (8192 STEP) PULSE WIDTH-RATE MULTIPLIER D/A CONVERTER FOR TUNING VOLTAGE. BUILT IN ANALOGUE SWITCH.
- CRT DISPLAY SECTION BASED ON A 64 x 64 FULLY PROGRAMMABLE MATRIX, UNDER SOFTWARE CONTROL, WORKS WITH ANY TV STANDARD
- OPEN DRAIN OUTPUTS RATED UP TO 13.2V
- MAIN 5V POWER SUPPLY (12V USED FOR BIAS)
- STANDARD 40 PIN PLASTIC PACKAGE

The M 106 is a programmable LSI device for microprocessor controlled applications in TV and industrial control fields. The M 106 uses state-of-the-art N-Channel MOS Silicon gate technology, with a single +5V power supply and TTL compatible inputs and outputs. A +12V supply is used for bias of the analogue switch circuit built on the chip.
The microprocessor interface includes a single phase clock input, a bidirectional 8 bit system bus, two strobe inputs and an interrupt request output. A total qf 7 variable duty cycle output signals are available. After simple RC filtering these signals become the analogue outputs of the system. One blanking and three colour outputs are provided to display alphanumeric or graphic data on a CTV screen. Eight general purpose digital outputs are provided with open-drain configuration.
The M 106 is available in a standard 40 pin dual-in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

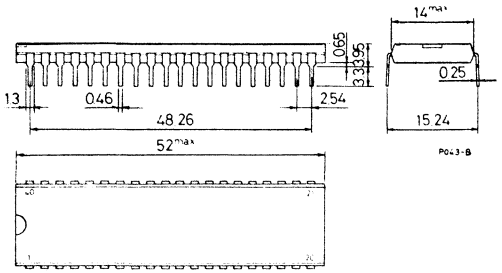
V_{DD} **	Supply voltage	-0.3 to 7	V
V_{ref}	Reference voltage	-0.3 to 7	V
V_{GG}	Bias voltage	-0.3 to 14	V
V_I	Input voltage	-0.3 to 7	V
$V_{O(off)}$	Off-state output voltage: P0 to P6; Q0 to Q7	-0.3 to 14	V
	all other outputs	-0.3 to 7	V
I_O	Output current: all outputs except pins 25, 26, 27, 28	max. 5	mA
	pins 25, 26, 27, 28	max. 15	mA
P_{tot}	Total package power dissipation	0.8	W
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
** All voltage are referred to $V_{SS1} = V_{SS2}$.

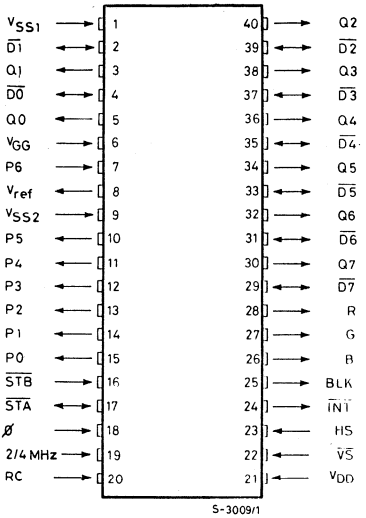
ORDERING NUMBER : M 106 B1

M 106

MECHANICAL DATA (dimensions in mm)



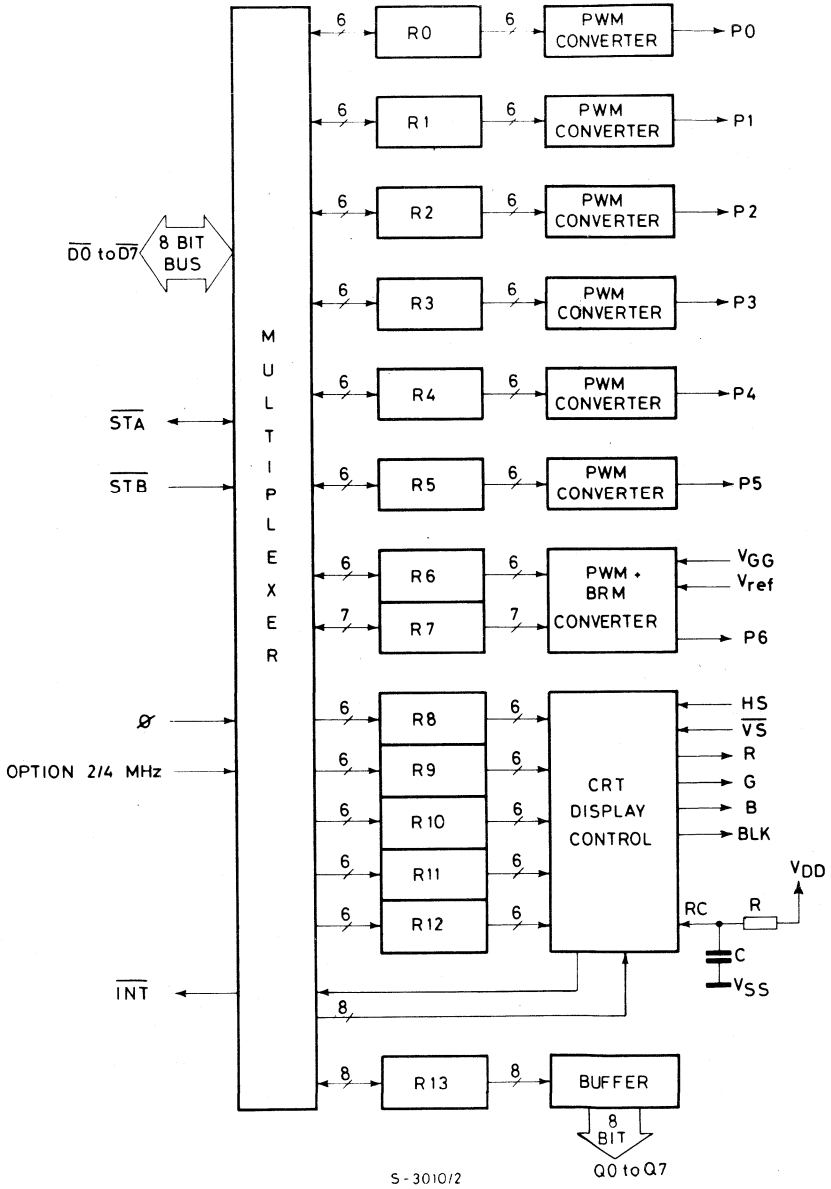
PIN CONNECTIONS



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	4.5 to 5.5	V
V_{ref}	Reference voltage	5 to 6	V
V_{GG}	Bias voltage	10.8 to 13.2	V
V_I	Input voltage	0 to V_{DD}	V
$V_{O(off)}$	Output off voltage: P0 to P6; Q0 to Q7	max 13.2	V
	all other outputs	max V_{DD}	V
I_O	Output current: all outputs except pins 25, 26, 27, 28	max 2	mA
	pins 25, 26, 27, 28	max 8	mA
ϕ	Clock frequency (selectable)	(pin 19 at V_{DD}) 2	MHz
		(pin 19 at V_{SS}) 4	MHz
f	Oscillator frequency	3.2	MHz
R	Resistance of the clock oscillator	2.2 to 10	kΩ
C	Capacitance of the clock oscillator	10 to 30	pF
T_{op}	Operating temperature	0 to 70	°C

BLOCK DIAGRAM



S-3010/2

STATIC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions

Typ. values are at T_{amb}= 25°C, V_{DD}= 5V; V_{Ref}= 5V; V_{GG}= 12V)

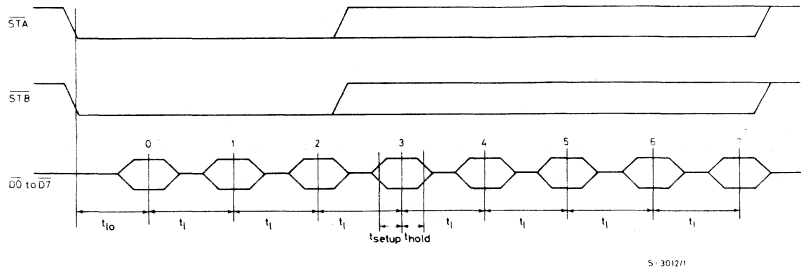
Parameter			Test conditions	Values			Unit
				Min.	Typ.	Max.	
V_{IH}	Input high voltage	All input pins except 22-23 (H_s-$\overline{V}_s$)		2.5		V_{DD}	V
		pins 22-23 (H_s-$\overline{V}_s$)		3		V_{DD}	
V_{IL}	Input low voltage	All inputs excepts pins 22-23 (H_s-$\overline{V}_s$))		0		0.8	V
		pins 22-23 (H_s-$\overline{V}_s$)		0		0.4	
I_I	Input leakage current	All inputs except pin 18	V_I = 0 to 5.5V			10	µA
I_ϕ	Input bias current	pin 18	V_ϕ = 5.5V	10		70	µA
V_{OL}	Output low voltage	All outputs except pins 25-26-27-28-7	I_{OL}= 1.6 mA			0.4	V
		pins 25-26-27-28	I_{OL}= 8 mA			1	V
		pin 7	I_{OL}= 0.25 mA		30	45	mV
V_{OH}	Output high voltage	pin 7	I_{OH}= -0.25 mA		V_{DD}-30	V_{DD}-45	mV
$I_{O(off)}$	Leakage current	All output except pins 3-5-25-26-27-28 30-32-34-36-38-40	$V_{O(off)}$= 5.5V			10	µA
		pins 3-5-25-26-27-28 30-32-34-36-38-40	$V_{O(off)}$= 13.2V			50	µA
I_{DD}	Supply current	pins 3-5-25-26-34	V_{DD}= 5.5V			60	mA
I_{GG}	Bias current		V_{GG}= 13.2V			300	µA

Note: The $\overline{V}_s$ and H_s inputs have Schmitt-trigger action for accepting slow transition time signals.

DYNAMIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
t_{I0}	Loading time of the first byte from the strobe display command ($\overline{STA}$ and $\overline{STB}$ both low)	see fig. 1		26		µs
t_I	Loading time of any successive byte from the end of the previous load time			24		µs
t_{setup}	Setup time			4		µs
t_{hold}	Hold time			4		µs

Fig. 1



DESCRIPTION

ϕ - System clock

The ϕ input (pin 18) must be connected to the microprocessor clock, or to the clock oscillator pin in the case where the microprocessor has a built in clock generator.
The clock signal can be 2 or 4 MHz. Pin 19 must be connected to V_{DD} if the frequency is 2 MHz, to V_{SS} if it is 4 MHz.

Internal registers load and read operations

M 106 can be fully programmed by loading a set of internal registers.
Table 1 shows the binary address code and function of each internal register.
The loading of each register, as shown by fig. 2, is performed in two steps: in the first phase, the four bit address code ($\overline{D0}$ to $\overline{D3}$) is sent on the bus, and latched by the $\overline{STA}$ strobe signal; in the second phase the bus carries the 6 to 8 bit register content which is transferred to the addressed register by the $\overline{STB}$ strobe signal.
When both $\overline{STA}$ and $\overline{STB}$ are in the HIGH state, the content of the addressed register will be read back to the bus. The read operation is not allowed for registers 8 to 12.

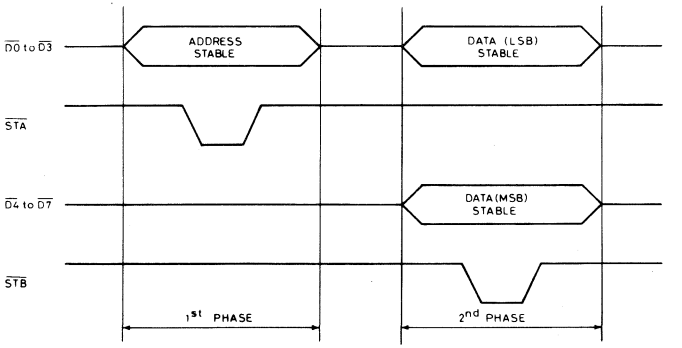
Table 1 - Summary of the internal registers

N°	ADDRESS $\overline{D3}$	$\overline{D2}$	$\overline{D1}$	$\overline{D0}$	Number of bit	Function
0	H	H	H	H	6	Converter n. 0 (PWM)
1	H	H	H	L	6	Converter n. 1 (PWM)
2	H	H	L	H	6	Converter n. 2 (PWM)
3	H	H	L	L	6	Converter n. 3 (PWM)
4	H	L	H	H	6	Converter n. 4 (PWM)
5	H	L	H	L	6	Converter n. 5 (PWM)
6	H	L	L	H	6	Converter n. 6 MSB (PWM)
7	H	L	L	L	7	Converter n. 7 LSB (BRM)
8	L	H	H	H	6	Window upper side position
9	L	H	H	L	6	Window lower side position
10	L	H	L	H	6	Window left side position
11	L	H	L	L	6	Window right side position
12	L	L	H	H	6	CRT display control
13	L	L	H	L	8	Open drain digital outputs
14	L	L	L	H	–	Reset (only for testing)
15	L	L	L	L	–	Not used

Table 2 - Loading and reading of the internal registers

$\overline{STA}$	$\overline{STB}$	Function
H	H	the content of the addressed register is read back (except for R8 to R12)
L	H	address loading
H	L	data loading
L	L	pattern loading for CRT display

Fig. 2



NOTE: TIMING IS NOT CRITICAL; EVERY µP HAS INSTRUCTION CYCLE LARGER THAN MINIMUM SET UP AND HOLD TIMES FOR THE SHOWN OPERATION.

S-3011/2

D/A converters for analogue controls

The 6 bit contents of registers 0 to 5, after a pulse-width conversion and external filtering, are used for analogue commands as volume, brightness, colour saturation, contrast, tone and fine tuning.
The pulse width modulated output has a fixed period of 64 microseconds and variable width. The output is open drain, can be filtered by a simple RC network and can be varied from 0V to the reference voltage (13.2V max) in $2^6 = 64$ steps.

Tuning voltage D/A converter

Registers 6 and 7 may be considered as a single 13 bit register. The corresponding outputs value is normally used as a tuning voltage for a varicap tuner. The conversion uses a double modulation system, in order to minimize the ripple after the filter. The 6 most significant bits (register 6) are converted using the same pulse width modulation technique as registers 0 to 5.
The 7 least significant bits (register 7) generate a series of pulses with variable width and frequency (bit rate multiplier).
This approach greatly reduces the amplitude of the low frequency components in the output voltage, and allows an easier and more efficient filtering.
The converter's output, P6, uses an internal analogue switch, operating in a push-pull mode, and switches a very precise reference voltage, which is connected to the V_{ref} pin.
The 0 volt level, in order to minimize the ground noise, is supplied through a dedicated pin V_{SS2}, that is externally connected to ground.
A 12V bias voltage must be connected to the V_{GG} pin in order to operate the output stage in the push-pull mode.

On screen display

The on-screen display interface uses a vertical sync signal applied to the $\overline{V}_S$ input and horizontal sync signal applied to the H_S input.
A "vertical clock" is internally generated by dividing the line frequency H_S by a number N which defines the height of the matrix element.
Assigning to N a value of 4/5/6 the height of the corresponding matrix element becomes 4/5/6 lines. The choice of one of these values of N will adapt the M 106 to display on any video standard.
An internal RC oscillator, synchronized by the H_S input, gives a "horizontal clock", whose period

DESCRIPTION (continued)

defines the width of the matrix element. The frequency must be adjusted in order to have a width equal to 1/64th of the actual width of the screen.

The data to be displayed on the screen is normally contained in a rectangular "window". Inside the window the BLK output generates a blanking signal, thus creating a black rectangular background for the image. Position, height and width of the window are programmable by loading in registers 8-9-10-11 a 6 bit position value of each side of the window. The value is calculated in terms of the number of vertical or horizontal clock pulses from an origin.

The origin (0, 0) corresponds to the trailing edge of the $\overline{V}_S$ and H_S pulses and is therefore located in the upper left corner of the screen.

Inside the M 106, a dual 64 bit shift register synchronized by the horizontal clock, repeats the same pattern over N lines using the first shift register, while the μP can load the second one with the new pattern to be used in the next lines. Afterwards the new pattern content is transferred in parallel into the first register. The loading of the second shift register is synchronized by the ϕ clock. This takes 8 sequential bytes, with the timing shown in fig. 1. The loading time for each byte is 24 microseconds.

The loading begins when both $\overline{STA}$ and $\overline{STB}$ go LOW. The corresponding state is decoded as a "strobe display" command.

If the "strobe display" state is terminated by the μP before the internal shift register is completely loaded, the remaining bits are zero-filled.

The display control register (12) defines the start and the end of the display function, the combination of the colour outputs enabled (and therefore the colour of the image) and the timing signals used during the load operation.

Table 3 shows the function of each bit of the display control register.

No timing signals are used if the pattern doesn't change from line to line of the display (vertical or horizontal bands). In this case the pattern can be loaded asynchronously only at the beginning, and will be automatically repeated until the window is completely scanned.

The timing signals must be enabled for displaying character, because the line pattern is variable and must be loaded in synchronism with the screen scan. The $\overline{STA}$ pin, normally used as a strobe input, becomes bidirectional and generates for each frame a single pulse, negative going, and approximately 45 microseconds long, N lines before the beginning of the window.

This signal is used by μP to initiate the first load operation.

The $\overline{INT}$ gives a series of pulses for each frame, with a period of N lines, starting N lines before the beginning of the window and stopping N lines before the end of the window.

During the $\overline{STA}$ output pulse no control register loading is permitted and only the "strobe display" state is accepted.

Table 3 - CRT display control register (N° 12)

Bit	Function	Logic level L	Logic level H
0	Output R (Red)	disabled	enabled
1	Output B (Blue)	disabled	enabled
2	Output G (Green)	disabled	enabled
3	Nr. of lines each dot	5 (4*)	6
4	Timing outputs $\overline{INT}$-$\overline{STA}$	disabled	enabled
5	Display control	stop	start

* Available with metal option (contact local SGS-ATES sales office).

MOS INTEGRATED CIRCUITS

M 108
M 208

PRELIMINARY DATA

SINGLE CHIP ORGAN (SOLO + ACCOMPANIMENT)

- SIMPLE KEY SWITCH REQUIREMENTS FOR 61 KEYS, IN A MATRIX OF 12 x 6
- LOW TIME REQUIRED FOR A SCANNING CYCLE OF 576 μsec.
- ACCEPTANCE OF ALL KEYS PRESSED
- TWO KEYBOARD FORMATS: 61 KEYS (SOLO) OR 24+37 (M108), 17+44 (M208) KEYS (ACC. + SOLO) WITH POSSIBILITY OF AUTOMATIC CHORDS OF THE "ACCOMPANIMENT" SECTION
- TOP OCTAVE SYTHESIZER INCORPORATED FOR GENERATION OF 3 "FOOTAGES"
- MORE THAN ONE CHIP CAN BE EMPLOYED WITH SYNCHRONIZATION THROUGH THE RESET INPUT
- SEPARATED ANALOG OUTPUTS (FOR EACH FOOT) FOR "SOLO", "ACC." AND "BASS" SECTIONS (SQUARE WAVE 50% D.C.) WITH AVERAGE VALUE CONSTANT
- INTERNAL ANTI-BOUNCE CIRCUITS
- KEY DOWN AND TRIGGER OUTPUTS FOR "SOLO", "ACC." AND "BASS" SECTIONS
- SUSTAIN FOR THE LAST KEYS RELEASED IN THE "SOLO" SECTION
- CHOICE OF OPERATING MODE IN "ACC." SECTION
  - MANUAL, WITH OR WITHOUT MEMORIZATION OF THE SELECTED KEYS (FREE CHORDS WITH ALTERNATE BASS)
  - AUTOMATIC, WITH OR WITHOUT MEMORIZATION OF THE SELECTED KEY (PRIORITY TO THE LEFT FOR AUTOMATIC CHORDS AND BASS ARPEGGIO)
- MULTIPLE CHOICE POSSIBILITY ON THE CHORDS IN AUTOMATIC MODE
  - MAJOR OR MINOR THIRD
  - WITH OR WITHOUT SEVENTH
- LOW DISSIPATION OF $\leqslant$ 600 mW
- STANDARD SINGLE SUPPLY OF +12V $\pm$ 5%
- INPUTS PROTECTED FROM ELECTROSTATIC DISCHARGES

The M108 and M208 are realized on a single monilithic chip using N-channel silicon gate technology. They are available in a 40 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Source supply voltage	-0.3 to +20	V
V_i **	Input voltage	-0.3 to +20	V
I_o	Output current (at any pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 50	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

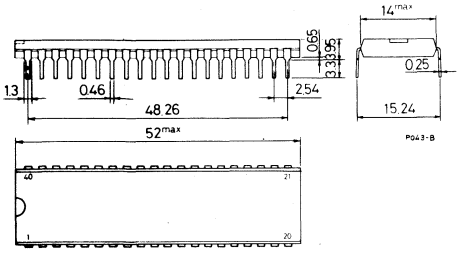
** This voltage is with respect to V_{SS} (GND) pin voltage.

ORDERING NUMBERS: M 108 B1 for dual in-line plastic package
M 208 B1 for dual in-line plastic package

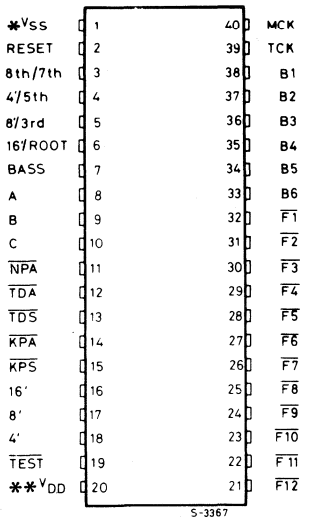
M 108
M 208

MECHANICAL DATA (dimensions in mm)

Dual in-line plastic package



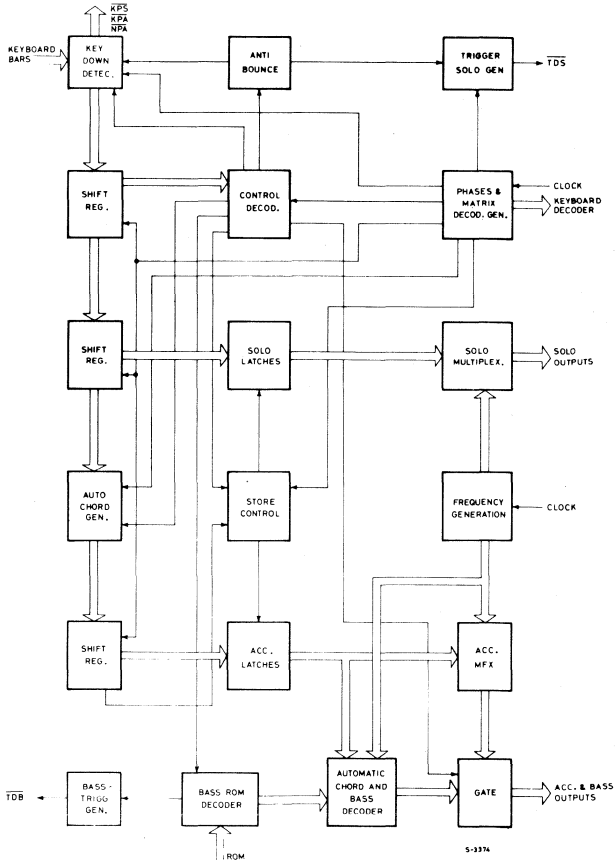
PIN CONNECTIONS



* V_{SS} is the lowest supply voltage

** V_{DD} is the highest supply voltage

BLOCK DIAGRAM



GENERAL CHARACTERISTICS

The caracteristics of the M208 are similar to those of the M108; the only difference is the keyboard split, which is 24+37 for the M108 and 17+44 for the M208 when used in "accompaniment + solo" mode.

The circuit comprises:

a) 2 pins for clock input: one for the matrix scanning, the other for the incorporated T.O.S.; by connecting both the clock inputs to the same matrix scanning clock (1000.12 KHz), the three "footages" generated are 16', 8' and 4'.

b) 6 inputs from the octave bars (keyboard and control scanning

c) 3 multiplexed data inputs for addressing the bass selection. These inputs normally come from the outputs of an external memory (negative or positive logic with control inside the chip)

d) 8 signal outputs divided by section: 3 for the "SOLO" section (16', 8', 4'), 4 for the "ACC." section (16' or root, 8' or 3rd, 4' or 5th, 8th/7th according to operating mode), 1 for the bass

e) 12 outputs for the matrix scanning

f) 5 "trigger" and "key down" outputs: $\overline{KPS}$ (key pressed "SOLO"), $\overline{TDS}$ (trigger decay "SOLO"), $\overline{KPA}$ (key pressed "ACC."), $\overline{NPA}$ (pitch present in "ACC." outputs), $\overline{TDB}$ (trigger decay "BASS") respectively. These outputs, in conjunction with an external time constant, allow the formation of the envelope of the sustain and percussion effects. The duration of the trigger pulses is $\cong$ 9 msec.

g) 1 input (reset) to synchronize the device or more than one device (with the same keyboard scanning and using a single contact per key).
The reset action, provided by an external circuit, is of the "POWER ON RESET" (high active) type and its duration must be $\cong$ 0.5 msec.

h) 1 $\overline{TEST}$ pin (in use it must be connected to V_{DD})

i) 2 supply pins.

MATRIX ORGANIZATION (Keyboard and controls)

M108/208 Matrix outputs	M108/208 Octave bar inputs					
	B_1	B_2	B_3	B_4	B_5	B_6
$\overline{F_1}$	C_1	C_2	C_3	C_4	C_5	C_6
$\overline{F_2}$	C_1#	C_2#	C_3#	C_4#	C_5#	7th OFF/7th ON
$\overline{F_3}$	D_1	D_2	D_3	D_4	D_5	3rd+/3rd-
$\overline{F_4}$	D_1#	D_2#	D_3#	D_4#	D_5#	Sust. OFF/Sust. ON
$\overline{F_5}$	E_1	E_2	E_3	E_4	E_5	$\overline{Latch}$/Latch
$\overline{F_6}$	F_1	F_2	F_3	F_4	F_5	Man/Auto
$\overline{F_7}$	F_1#	F_2#	F_3#	F_4#	F_5#	61/24 + 37 (17 + 44)
$\overline{F_8}$	G_1	G_2	G_3	G_4	G_5	Antibounce ON/Antibounce OFF
$\overline{F_9}$	G_1#	G_2#	G_3#	G_4#	G_5#	ROM Low/ROM High
$\overline{F_{10}}$	A_1	A_2	A_3	A_4	A_5	————
$\overline{F_{11}}$	A_1#	A_2#	A_3#	A_4#	A_5#	————
$\overline{F_{12}}$	B_1	B_2	B_3	B_4	B_5	————

C_1 is the first key on the left, C_6 is the last key on the right of the keyboard.

The main feature of this chip is the possibility of formating the keyboard either with 61 keys (only "SOLO" without automatism) or separating it into two sections ("ACCOMPANIMENT + SOLO") with the possibility of chord and bass automatic in the first section.

FEATURES

a) The "61/24 + 37" (17 + 44) control chooses the keyboard operating mode, i.e. the whole keyboard dedicated to "SOLO" or 24 (17) keys dedicated to "ACCOMPANIMENT" and 37 (44) to "SOLO".

b) The "Man/Auto" control, which operates only in case of "ACC.+ SOLO", chooses the manual or the automatic accompaniment.

c) The "Sust OFF/Sust ON" allows the storage of the "SOLO" section and handles the whole keyboard or 37 (44) keys depending on the operating mode.

d) The "$\overline{\text{Latch}}$/Latch" similarly allows the storage of the "ACC." section and operates in "ACC.+ SOLO" only.

e) The "3rd+/3rd-" which operates only in case of "ACC.+ SOLO" and "AUTOMATIC", changes the automatic chord generated from major to minor or viceversa.

f) The "7th OFF/7th ON" adds the seventh to the automatic chord generated.

g) The "Antibounce ON/Antibounce OFF" disables the antibounce circuit which is usually enabled.

h) The "ROM Low/ROM High" selects between ROMs with return to "1" (Low active) or with return to "0" (High active). Usually the chip is enabled for ROMs with return to "1" (Low active).

"SOLO" Operation

In this case the chip recognizes the whole keyboard as "SOLO" and does not read the controls which concern the "ACC.+ SOLO" operation.
The chip identifies all the keys pressed and transfers to the outputs of each section (ACC. and SOLO) the analog sum of corresponding pitches.
The outputs are current generators with average value constant, therefore it is sufficient to connect the pins to one load and send the signals on to the filters.
In the case of "Sustain OFF" each new key pressed or released is accepted or deleted in a time $\leqslant 576\ \mu$sec.
In the case of "Sustain ON" the chip has a different operation according to whether the new key (keys) is pressed or released: each new key pressed is always accepted in a time $\leqslant 576\ \mu$sec., whereas each key released is deleted with a delay of 73 msec. and only if there are still keys pressed.
In fact, if after the 73 msec. there are no keys pressed, the last key (or keys) released remains stored until new keys are pressed.
In this mode it is possible to have Sustain, with external envelope shaping, for the last keys (or key) released.
The pitch envelope is controlled by a D.C. signal $\overline{\text{KPS}}$ (any key pressed) and there is also an A.C. signal $\overline{\text{TDS}}$ (trigger decay "SOLO") which provides a pulse whenever a key is pressed.
An appropriate antibounce circuit, inside the chip, solves the problems associated with the keyboard contacts.

"SOLO + ACCOMPANIMENT" Operation

In this case the chip identifies the "ACCOMPANIMENT" on the first 24 (17) keys on the left, and the "SOLO" on the remaining 37 (44) keys and reads all the controls which concern the "ACC." section. The "SOLO" function is identical to "61 keys" mode, but for the "ACC." section there are two possibilities:

A) **MANUAL**
The chip identifies which keys are pressed in the "ACC." section, and transfers to the "ACC." outputs the analog sum of the corresponding pitches.
The "ACC." section is fully independent of the "SOLO" section and the signals (if there is no "LATCH") remain at the output only while the keys are pressed even if there is "SUSTAIN ON".

The "BASS" section gives at the bass output an alternating bass between the first on the left and the first on the right of the keys pressed in the "ACC." section; the pitch switching timing is dependent on an external ROM (3 bits).
The "LATCH" control stores the last keys released and the output signals, including the bass output, remain until new keys are pressed.
The $\overline{TDB}$ (trigger decay "BASS") output gives a pulse corresponding to every output change; there are also two D.C. signals, $\overline{KPA}$ (any key pressed accompaniment) and $\overline{NPA}$ (pitches in output accompaniment) relative only to the "ACC." section.
The first of these signals (analogous to $\overline{KPS}$) concerns the keyboard and does not consider the "LATCH" condition.
The second on the contrary concerns the "ACC." output and considers the "LATCH" condition.

B) **AUTOMATIC**

The chip recognizes in the "ACC." section only the first on the left of the keys pressed and, according to the setting of the following controls, produces a major or minor chord with or without seventh only the 4' footage but with separated outputs for root, third, fifth and eighth (or seventh if the chord is with seventh).
The bass section gives the bass arpeggio among root, third, fourth, fifth, sixth, seventh and eighth with pitch switching dependent on an external ROM (3 bits).
In automatic mode the two octaves of the "ACC." section inside the chip are connected in parallel both for the chord and for the bass; therefore by pressing anyone of the two keys of the same note the chip generates the same chord.
The "LATCH" control stores the major chord and the bass pitches (until new keys are pressed); the modification of the chord stored (from major to minor, addition of seventh) is always possible by operating the proper controls: by releasing these controls the chord becomes major again.
It is possible to delete the stored pitches both is manual and in "AUTOMATIC" mode by a $\overline{Latch}$ control signal.
Once again there are $\overline{KPA}$, $\overline{NPA}$, and $\overline{TDB}$ information; however the $\overline{TDB}$ pulse, which normally appears at each arrival of the ROM codes, does not appear if there are no pitches in the "ACC." (and bass) outputs or, in the case of alternate bass (in manual mode) if the codes indicate conditions of indifference.

RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{SS}	Lowest supply voltage		0		0	V
V_{DD}	Highest supply voltage		11.4	12	12.6	V

BASS TRUTH TABLES

LOW ACTIVE

External Memory Code			Bass Arpeggio Output (Automatic mode)	Alternate Bass Output (Manual mode)
C	B	A		
1	1	1	No change	No change
1	1	0	Root	1st on the left
1	0	1	3rd	– – –
1	0	0	4th	– – –
0	1	1	5th	1st on the right
0	1	0	6th	– – –
0	0	1	7th	– – –
0	0	0	8th	– – –

HIGH ACTIVE

External Memory Code			Bass Arpeggio Output (Automatic mode)	Alternate Bass Output (Manual mode)
C	B	A		
0	0	0	No change	No change
0	0	1	Root	1st on the left
0	1	0	3rd	– – –
0	1	1	4th	– – –
1	0	0	5th	1st on the right
1	0	1	6th	– – –
1	1	0	7th	– – –
1	1	1	8th	– – –

STATIC ELECTRICAL CHARACTERISTICS (Positive Logic, V_{DD}= +10 to +14V, V_{SS}= 0V, T_{amb}= 0 to 50°C unless otherwise specified)

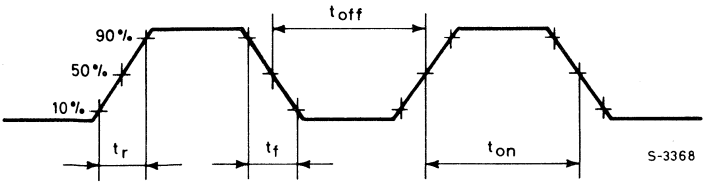
Parameter		Test conditions	Min.	Typ.	Max.	Unit
INPUT SIGNALS						
V_{IH}	Input high voltage	Note 1	V_{DD}-1		V_{DD}	V
		Note 2	4		18	V
		Note 3	V_{DD}-2		V_{DD}	V
V_{IL}	Input low voltage	Note 1	V_{SS}		V_{SS}+1	V
		Note 2	V_{SS}		V_{SS}+0.6	V
		Note 3	V_{SS}		V_{SS}+2	V
I_{LI}	Input leakage current	V_I= +14V T_{amb}= 25°C			10	µA
LOGIC SIGNAL OUTPUTS						
R_{ON}	Output resistance with respect to V_{SS}			300	500	Ω
R_{ON}	Output resistance with respect to V_{DD}	V_{OUT}= V_{DD}-1 (driver off)		15	25	kΩ
V_{OH}	Output high voltage		V_{DD}-0.4		V_{DD}	V
V_{OL}	Output low voltage			V_{SS}+0.2	V_{SS}+0.4	V
POWER DISSIPATION						
I_{DD}	Supply current	T_{amb}= 25°C		30	45	mA
ANALOG SIGNAL OUTPUTS (the external load must be connected to $V_{DD}/2$)						
I_{OH}	Output current with respect to $V_{DD}/2$	Outputs loaded with 1 KΩ resistor versus $V_{DD}/2$	35	50	70	µA
I_{OL}	Output current with respect to V_{SS}	Outputs loaded with 1 KΩ resistor versus $V_{DD}/2$	-35	-50	-70	µA

Note 1 : Refers only to the clock inputs.
Note 2 : Refers only to the inputs from the external memory.
Note 3 : Refers only to the reset input.

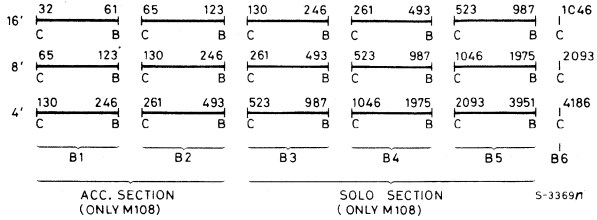
DYNAMIC ELECTRICAL CHARACTERISTICS

Parameter		Test conditions	Min.	Typ.	Max.	Unit
MASTER CLOCK INPUT						
f_i	Input clock frequency			1000.12		KHz
t_r, t_f	Input clock rise and fall time 10% to 90%	1000.12 KHz			40	ns
t_{on}, t_{off}	Input clock ON and OFF times	1000 KHz		500		ns
T.O.S. CLOCK INPUT						
f_i	Input clock frequency		100	1000.12	2500	KHz
t_r, t_f	Input clock rise and fall times 10% to 90%	1000.12 KHz			40	ns
t_{on}, t_{off}	Input clock ON and OFF times	2000 KHz		250		ns
$\overline{TDS}$ and $\overline{TDB}$ OUTPUTS						
t_{on}	Pulse duration	1000 KHz		9.216		ms
t_r, t_f	Outputs rise and fall times 10% to 90%	1000 KHz		100		ns

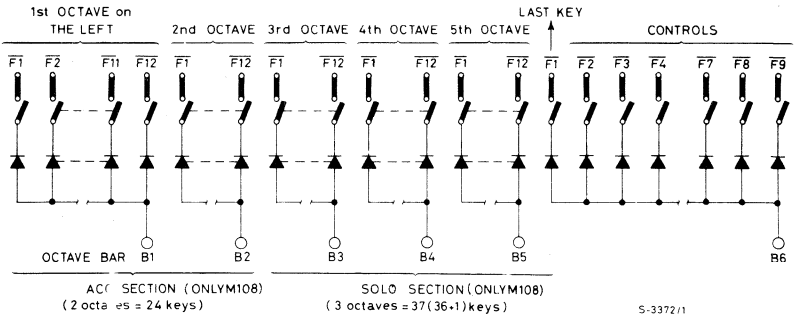
INPUT CLOCK WAVEFORM



FREQUENCY RANGE OF EACH OCTAVE (16', 8', 4' footages)

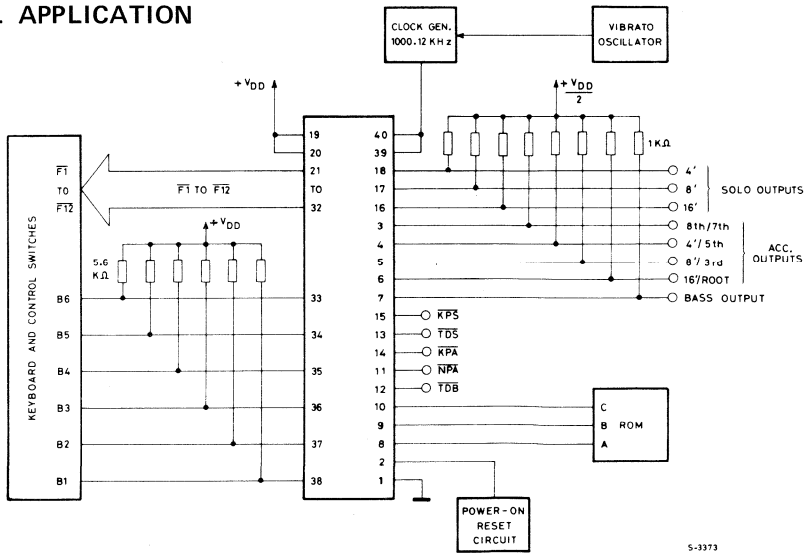


CONNECTION OF THE KEYBOARD AND CONTROL SWITCHES

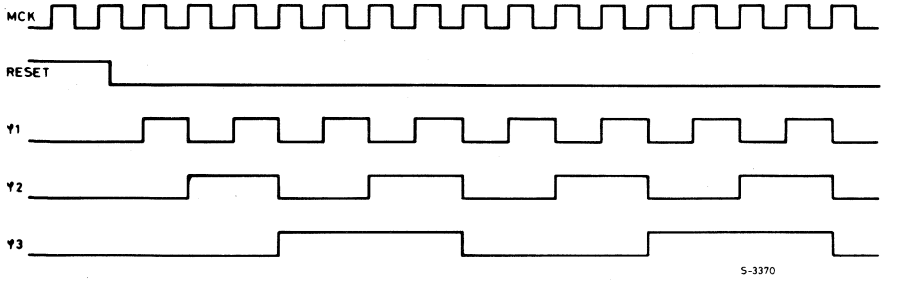


Note: The switch "OPEN" corresponds to "KEY NOT PRESSED" or "CONTROL IN THE FIRST CONDITION" (see the drawing "MATRIX ORGANIZATION").

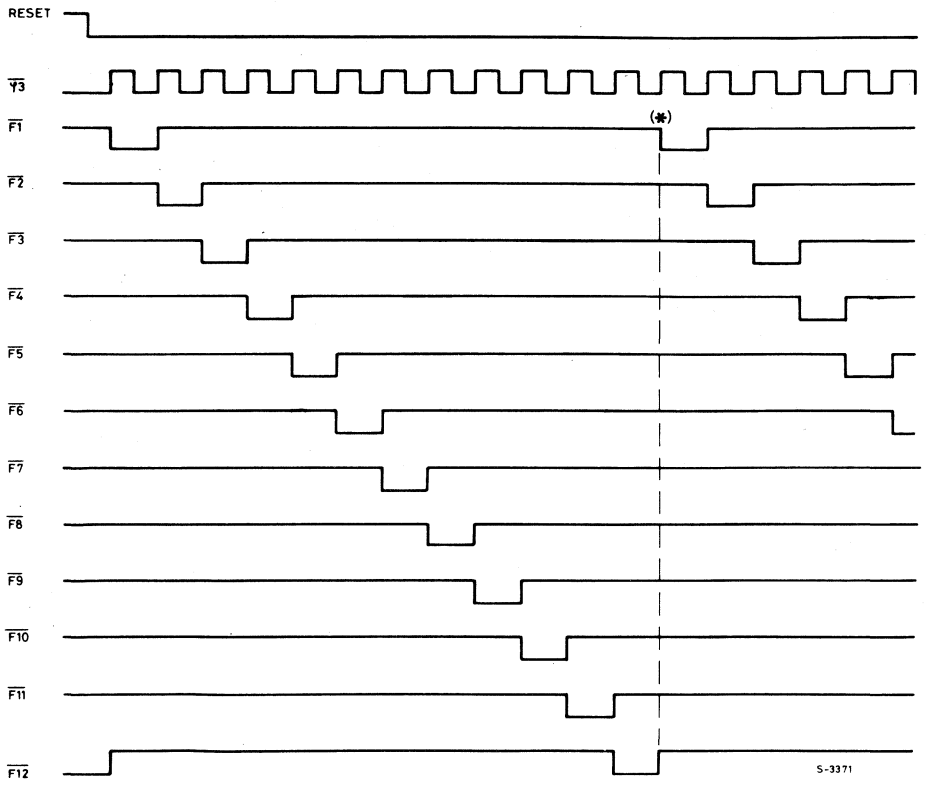
TYPICAL APPLICATION



TIMING DIAGRAMS



Note: MCK is the master clock input (matrix scanning), $\varphi 1$, $\varphi 2$, $\varphi 3$ are internal phases to generate $\overline{F1} \div \overline{F12}$.



Note: The matrix scanning starts (after the power on reset) at the second arrival in output of $\overline{F1}$ (*) from B1 to B6 in continuous sequence.

MOS INTEGRATED CIRCUIT

M 110

PRELIMINARY DATA

MONOPHONIC SYNTHESIZER

- LOW POWER DISSIPATION < 500 mW TYP.
- N-CHANNEL SILICON GATE PROCESS
- DIGITAL PORTAMENTO EFFECT
- EXTERNAL CONTROL (WITH RC) OF THE PORTAMENTO SPEED IN THE 100 μs to 150 ms RANGE FOR EACH HALF TONE
- EXTERNAL OSCILLATOR FOR PORTAMENTO (EXT. OSC.)
- STANDARD SUPPLY (12V, GND)
- MATRIX ORGANIZATION 12 x 6 WITH 61 POSITIONS FOR THE KEYBOARD AND 6 COMMANDS
- RESET INPUT FOR FREQUENCY CLAMP
- PRIORITY LEFT OR RIGHT OF THE PRESSED KEYS
- 3 CODED OUTPUTS FOR THE OCTAVE INFORMATION OF THE PLAYING FREQUENCY
- 2 TRIGGER SIGNALS $\overline{TP}$ AND $\overline{TS}$ FOR PERCUSSION AND KEY PRESSED
- 1 OUTPUT WITH DC CURRENT PROPORTIONAL TO THE PLAYING FREQUENCY
- 1 OUTPUT WITH PULSE FOR FALLING EDGE OF THE EXTERNAL SAWTOOTH WAVEFORM (20 μs)
- SAWTOOTH WAVEFORM SELECTABLE (4', 8', 16', 32')
- PROVISION FOR OBTAINING SAWTOOTH WAVEFORMS WITH FEW EXTERNAL COMPONENTS ON THE 4', 8', 16', 32' FOOTAGES
- 1 OUTPUT WITH FOOT AND DUTY CYCLE ON FOLLOWING COMMANDS
- 4 OUTPUTS WITH 50% DUTY CYCLE (2', 4', 8', 16')

The M110 is realized on a single monolithic silicon chip using low threshold N-channel silicon gate MOS technology. It is available in a 40 lead plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.3 to 20	V
V_I	Input voltage	-0.3 to 20	V
I_o	Output current (at any output pin)	3	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 50	°C

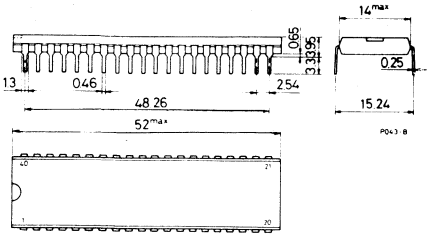
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

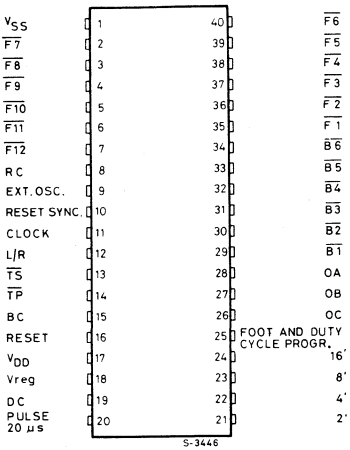
ORDERING NUMBER: M110 B1 for dual in-line plastic package

MECHANICAL DATA (dimensions in mm)

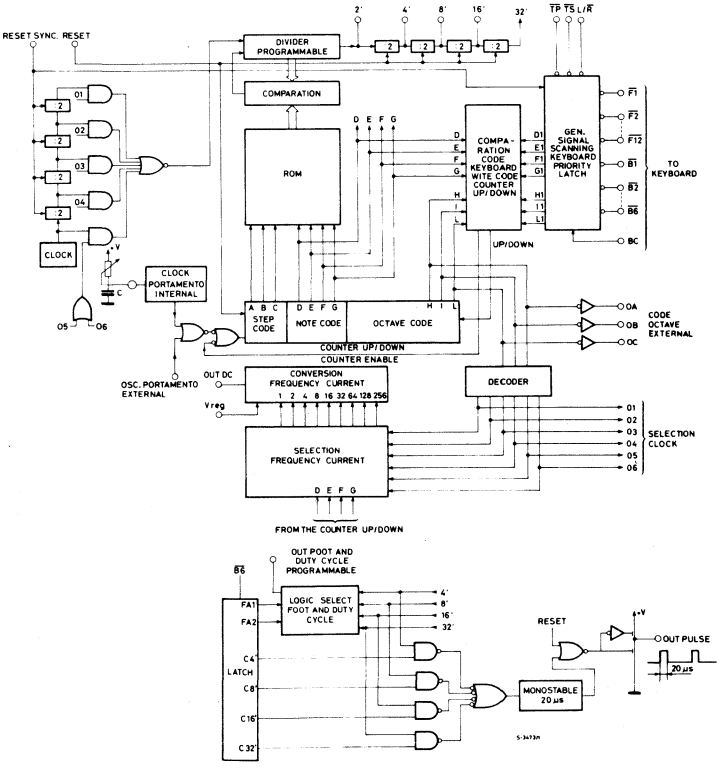
Dual in-line plastic package (40 lead)



PIN CONNECTIONS



BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (V_{DD} = 12V ± 5%, V_{SS} = 0V, T_{amb} = 0 to 50°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK INPUT (pin 11)						
V_{IH}	Clock high voltage		V_{DD}-1		V_{DD}	V
V_{IL}	Clock low voltage		V_{SS}		V_{SS}+1	V
DATA INPUTS (pin 9, 10, 12, 15, 16, 29, 30, 31, 32, 33, 34)						
V_{IH}	Input high voltage		V_{DD}-2		V_{DD}	V
V_{IL}	Input low voltage		V_{SS}		V_{SS}+2	V
I_L	Input leakage current	V_i = 12.6V T_{amb} = 25°C			10	μA
DATA OUTPUTS (pin 13, 14, 21, 22, 23, 24, 25, 26, 27, 28) (2, 3, 4, 5, 6, 7, 35, 36, 37, 38, 39, 40 with external pull-up)						
R_{OUT}	Output res. to V_{SS} Output res. to V_{DD}	for V_o = V_{DD} - 1 (driver OFF)		300 15	500 25	Ω KΩ
V_{OH}	Output high voltage		V_{DD}-0.4		V_{DD}	V
V_{OL}	Output low voltage			V_{SS}+0.2	V_{SS}+0.4	V
POWER DISSIPATION						
I_{DD}	Supply current	T_{amb} = 25°C		30	50	mA
INTERNAL OSCILLATOR (pin 8)						
RC external		C = 4.7 nF R = 2.2MΩ(*) C = 4.7 nF R = 1 KΩ(*)		0.07 125		KHz
OUTPUT PULSE 20 μs (pin 20)						
V_{OH}	Output high voltage	I_{OH} = 0	8	9		V
V_{OL}	Output low voltage	I_{OL} = 300 μA	V_{SS}		V_{SS}+0.3	V
R_{OUT}	Output res. to V_{SS} Output res. to V_{DD}	for V_o = 6V		0.5 5	1 8	KΩ

(*) Max. admissible value of R = 2.2 MΩ; min. admissible value of R = 1 KΩ.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{DD} = 12V ± 5%, V_{SS} = 0V, T_{amb} = 0 to 50 °C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
CLOCK INPUT (pin 11)						
f_i	Input clock frequency		1600	2000.240	2500	KHz
t_r, t_f	Input clock rise and fall time 10 to 90%				40	ns
t_{on}, t_{off}	Input clock ON and OFF times	2 MHz	200	250		ns

GENERAL CHARACTERISTICS

The circuit includes:

Pin 2, 3, 4, 5, 6, 7, 35, 36, 37, 38, 39, 40

$\overline{F1}$ to $\overline{F12}$: outputs for selection of notes with 22 KΩ external pull-up. The maximum allowable external capacity must be < 500 pF. When not selected these outputs are at the high state (+12V).

Pin 29, 30, 31, 32, 33, 34

$\overline{B1}$ to $\overline{B6}$: inputs for selection of octave with 5.6 KΩ external pull-up so that these are at the high state when not selected.

Pin 12

L/R input for selecting priority to the left or right.

- if priority to the right is selected the note relative to the key farthest to the right of those pressed is supplied at the output
- priority to the left gives the possibility of choosing one key out of the first 12 pressed, starting from the left
- the internal pull-up is between 200 and 350 KΩ.

Pin 15

BC: input for selecting priority key in the case of priority to the left.

Pin 11

Clock: input frequency for generating notes.
(The internal logic of the system provides a precision equal to that of the TOS-M087-M083).

Pin 9, 8

Ex Osc-RC of Clock for portamento:

- an external oscillator with square wave can be connected at the first input (pin 9) limiting the max. frequency to 160 KHz. The duty cycle can be as desired provided that the minimum duration of the "0" and of the "1" is 2 μs.
- the 2nd input (pin 8) foresees the use of an external RC with the possibility of varying the frequency of the internal oscillator by regulating R.
  The maximum frequency value which can be measured on the pin must have a period T = 6 μsec. With values of R= 2.2 MΩ (potentiometer) and C = 4.7 nF, we obtain $T_{min} \simeq 8$ μs and $T_{max} \simeq 14$ ms. The corresponding portamento time between the 2 keys at the two extremes of the keyboard is: min. time ≃ 7 ms, max. time ≃ 12 sec.
- the portamento time between 2 semitones can be defined by applying the following formula:

  Portamento time = 16 x oscillator frequency period

  The two oscillators must not be switched on simultaneously; use of one must exclude the other. The pin for the oscillator not in use is connected to V_{SS}.
- The portamento time between 2 keys is proportional to the distance between them; this means that the law of portamento/keys variation is linear.

GENERAL CHARACTERISTICS (continued)

Pin 10

Reset Sync.: input required when several SGS-ATES devices are used, all having the same type of scanning, so that only one contact need be used per key. Ohterwise it is connected to V_{SS}.

Pin 16

Reset input (active high) active on outputs 2', 4', 8', 16', output with foot duty cycle programmable, output pulse 20 μs.

Pin 28, 27, 26

OA-OB-OC: used in binary code of the octave to which the note selected belongs. The highest weight code is relative to the lowest octave. The 3 outputs are of the push-pull type.

Pin 25

Output with foot and duty cycle programmable; digital output with possibility of 4 functions: 8', 12.5%, 8' 25%, 16' 6.25%, 16' 12.5%.
Only one function can be selected at a time with the commands inserted in the matrix of the keyboard (push-pull).

Pin 20

Output 20 μs pulse: output for zeroing the sawtooth whose duration is between 16 and 24 μs at 2 MHz of clock (push-pull).

Pin 13

$\overline{TS}$: output of key pressed: high in absence of keys pressed, low in presence of keys pressed (push-pull).

Pin 14

$\overline{TP}$; output of priority key; high in absence of keys inserted, low in priority conditions (in this case the output goes to zero for a time equal to 8 ± 0.6 ms with clock 2 MHz) (push-pull).

– The conditions required to make a pulse appear at this exit are:
a) insertion of at least 1 key
b) insertion of a new priority key
c) release of a priority key when another key pressed previously acquires priority.

Pin 21, 22, 23, 24

2'-4'-8'-16': square wave outputs (push-pull) with 50% of duty cycle on 4 different footages: 2', 4', 8', 16' corresponding to the following max frequencies: 8372 Hz; 4186 Hz; 2093 Hz; 1046 Hz.
These outputs switch on the rise front.

Pin 19

DC: output which generates a current proportional to the frequency output therefore exponential with the position of the key.

Pin 18

Vreg: input necessary for calibration of current (OUT DC) and amplitude of sawtooth for different devices.

GENERAL INFORMATION

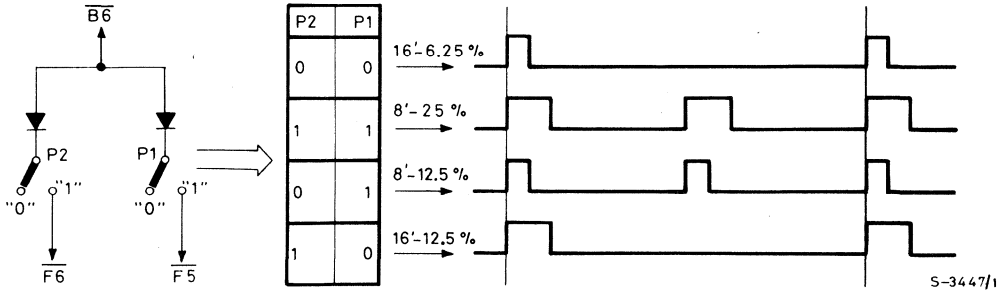
- Updating of a key between insertion and relative output information occurs in 0.5 ms.
- On release of all the keys pressed the last key released in order of time is memorized: consequently the relative frequency (on the 4 footages) and current (OUT DC) are memorized at the output.
- Each internal between 2 adjacent semitones is divided into 8 frequencies.
- The ratio between two contiguous frequencies is $\simeq \sqrt[96]{2}$.

Binary representation of octave codes

OA	OB	OC	
1	1	1	lowest octave
0	1	1	
1	0	1	
0	0	1	
1	1	0	
0	1	0	highest octave

Function with selectable foot and duty cycle

Selection of one of the 4 possible functions occurs via commands connected to the diode matrix of the keyboard.

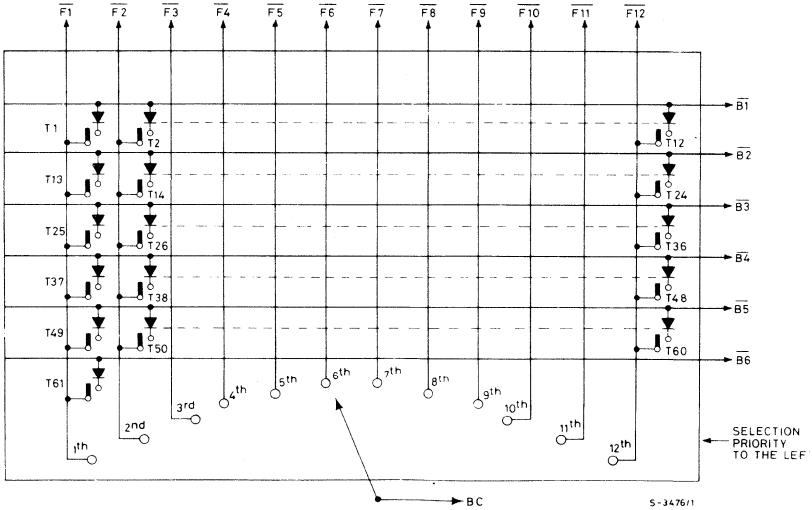


MATRIX ORGANIZATION (Keyboard and controls)

M110 matrix output	M110 Octave bar inputs						Selection for the priority on the left
	$\overline{B1}$	$\overline{B2}$	$\overline{B3}$	$\overline{B4}$	$\overline{B5}$	$\overline{B6}$	BC
$\overline{F1}$	(*) C1	C2	C3	C4	C5	(*) C6	1st key on the left
$\overline{F2}$	C1#	C2#	C3#	C4#	C5#		2nd key on the left
$\overline{F3}$	D1	D2	D3	D4	D5		3rd key on the left
$\overline{F4}$	D1#	D2#	D3#	D4#	D5#		4th key on the left
$\overline{F5}$	E1	E2	E3	E4	E5	P1 (***)	5th key on the left
$\overline{F6}$	F1	F2	F3	F4	F5	P2 (***)	6th key on the left
$\overline{F7}$	F1#	F2#	F3#	F4#	F5#		7th key on the left
$\overline{F8}$	G1	G2	G3	G4	G5		8th key on the left
$\overline{F9}$	G1#	G2#	G3#	G4#	G5#	(**) sawtooth 32'	9th key on the left
$\overline{F10}$	A1	A2	A3	A4	A5	(**) sawtooth 16'	10th key on the left
$\overline{F11}$	A1#	A2#	A3#	A4#	A5#	(**) sawtooth 8'	11th key on the left
$\overline{F12}$	B1	B2	B3	B4	B5	(**) sawtooth 4'	12th key on the left

(*) C1 is the first key on the left; C6 is the last key on the right of the keyboard.
(**) This control selects the correct pulse of the sawtooth generated by OUT DC (pin n° 19).
(***) P1 and P2 are the controls for the output with foot and duty cycle programmable.

12 x 6 MATRIX



If the device is used with selection of the first key to the left connect the control bar BC to V_{SS}.
For different priorities of the first key to the left connect BC to the selection frequency for the selected priority key. In this case BC must have a pull-up of 5.6 KΩ.
The selection sequence is: $\overline{F1}$ selects the first key to the left.

⋮

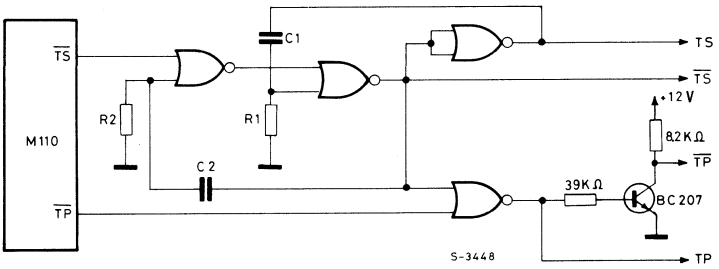
$\overline{F12}$ selects the twelfth key to left.

POWER ON RESET

The device must have an external circuit for the power-on reset (pin 16) high active. In the application diagram a power-on reset time of 0.5 sec is used and the circuit also connects, when active, the $\overline{B1}$ bar to V_{SS}.

ANTIBOUNCE CIRCUIT

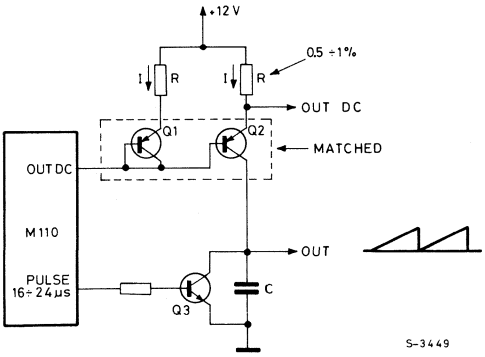
The antibounce circuit eliminates bounce caused by the contact springs of the keyboard. The bounce may supply wrong information at outputs $\overline{TS}$ and $\overline{TP}$.
The diagram is as follows:



The antibounce time can be regulated by acting on constants R1-C1 (antibounce on pressing a key) and R2-C2 (antibounce on release of key). In the application diagram of the device an antibounce of 18 ms is established C1 = C2 = 18 nF and R1 = R2 = 1 MΩ. The time constants must not however be 12 ms.
The antobounce circuit supplies the high or low active priority key and key pressed outputs compatible with the technical requirements requested.

GENERATION OF SAWTOOTH

The four sawtooth signals (4', 8', 16', 32' corresponding, for the last key on the right, to 4186 Hz; 2093 Hz; 1046 Hz, 523 Hz) are analog and are obtained by loading (with constant current) and unloading four external capacitors. A current mirror of the type shown below is produced.



- The reference of the sawtooth is V_{SS}.
- The best results are obtained using T1 and T2 matched with h_{FE} high while resistances R must have 0.5 to 1% precision.
  The maximum variation in the amplitude of the sawtooth (over the whole keyboard) is ± 4%.

CALIBRATION

a) Press key 61.

b) Regulate Vreg until OUT DC is 9V (± 3%).

c) In these conditions the sawtooth assumes an amplitude of 4V and Vreg= 5V ± 30%.

d) In these conditions value of R must be 1600 Ω.

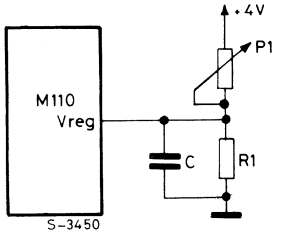
e) The OUT DC voltage must not fall below 9V (± 3%); this means that the maximum voltage excursion between the 1st and 61st key is 3V.

f) If OUT DC excursions lower than 3V are required for the whole keyboard, the value of R must be reduced in proportion to the new value of OUT DC.
let us consider come practical values of OUT DC:

OUT DC	R
3 V	1600 Ω
2 V	1066 Ω
1.5 V	800 Ω

values of R proportional to OUT DC

- This rule must be applied to avoid frequency/voltage linearity errors.
- The value of R must be between 100 to 1600 Ω.
- The current/frequency conversion and therefore the variation in amplitude of the sawtooth for the whole keyboard have a precision of 4%.
- When the value of R and the maximum value of OUT DC have been established the latter can be maintained constant for any device simply by acting on Vreg.
- The resistive divider from which the Vreg is taken should be established respecting the following rules:
  1) P1//R1 < 5 KΩ
  2) $\frac{P1\ max}{R1} = 4$ to 5

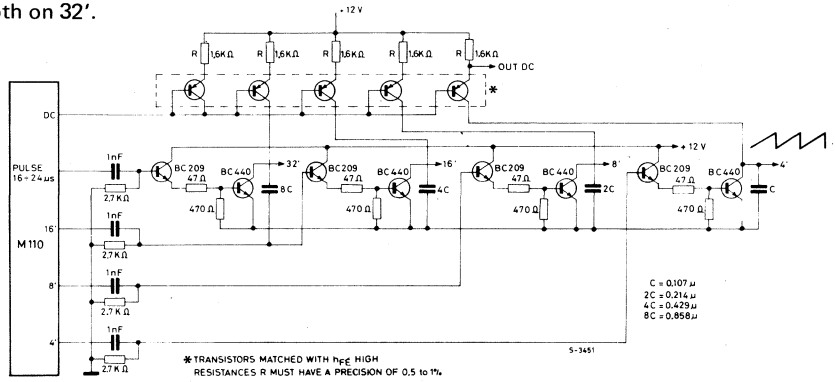


The values suggested for the four capacitances are respectively:

4'C = 0.107 μF; 9'C = 0.214 μF; 16'C = 0.429 μF; 32'C = 0.858 μF.

Outputs with simultaneous sawtooth on footages 4', 8', 16', 32'

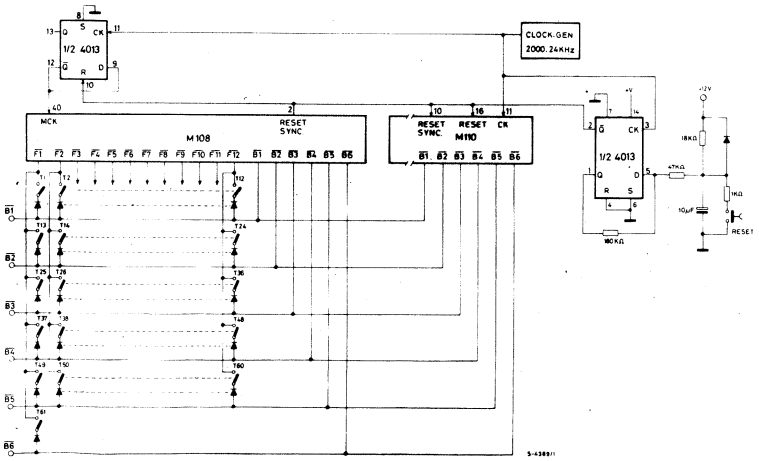
- The sawtooth can also be obtained simultaneously on 4 different footages: the diagram to be used is shown below.
- The zeroing pulses for 4', 8', 16' pulses are obtained by means of the rising fronts of the relative square wave outputs; for 32' however the 20 μs pulse is used, with the command for selection of the sawtooth on 32'.



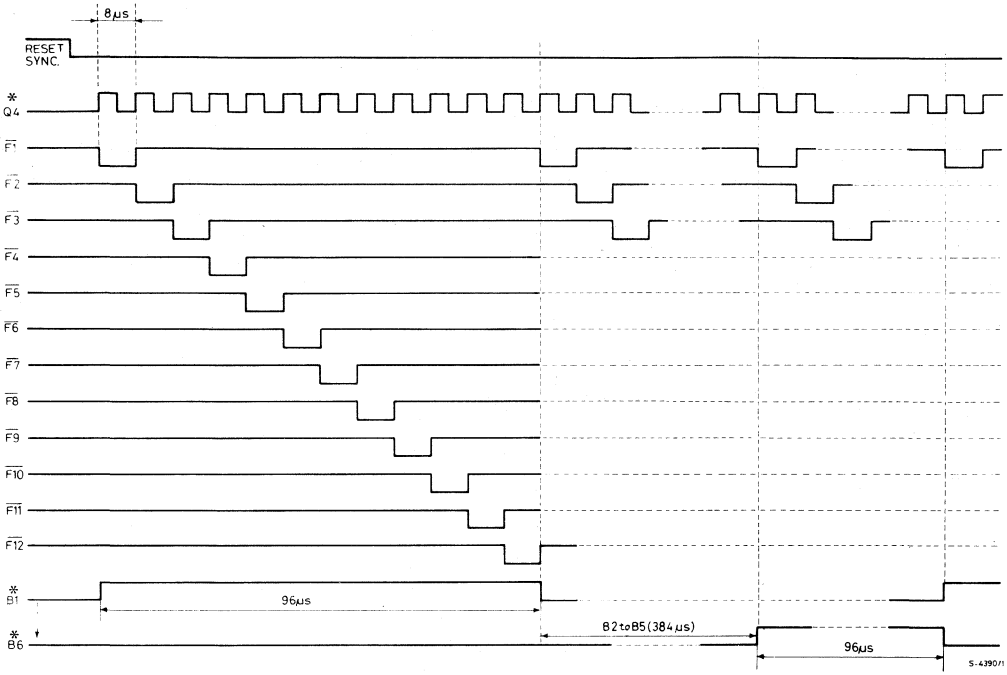
USE OF THE M108 AND M110 SIMULTANEOUSLY WITH ONLY ONE CONTACT FOR KEY

Application

The M108 and the M110 have the same connection with the keyboard therefore only one contact per key is sufficient to drive both the devices: one is the master, with outputs $\overline{F1}$ to $\overline{F12}$ connected to the keyboard switches, the other is the slave and will receive the information in bus $\overline{B1}$ to $\overline{B6}$ together with the master.
The synchronization is made by the reset (sync.) pin.

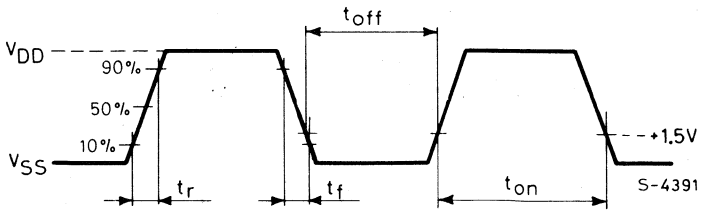


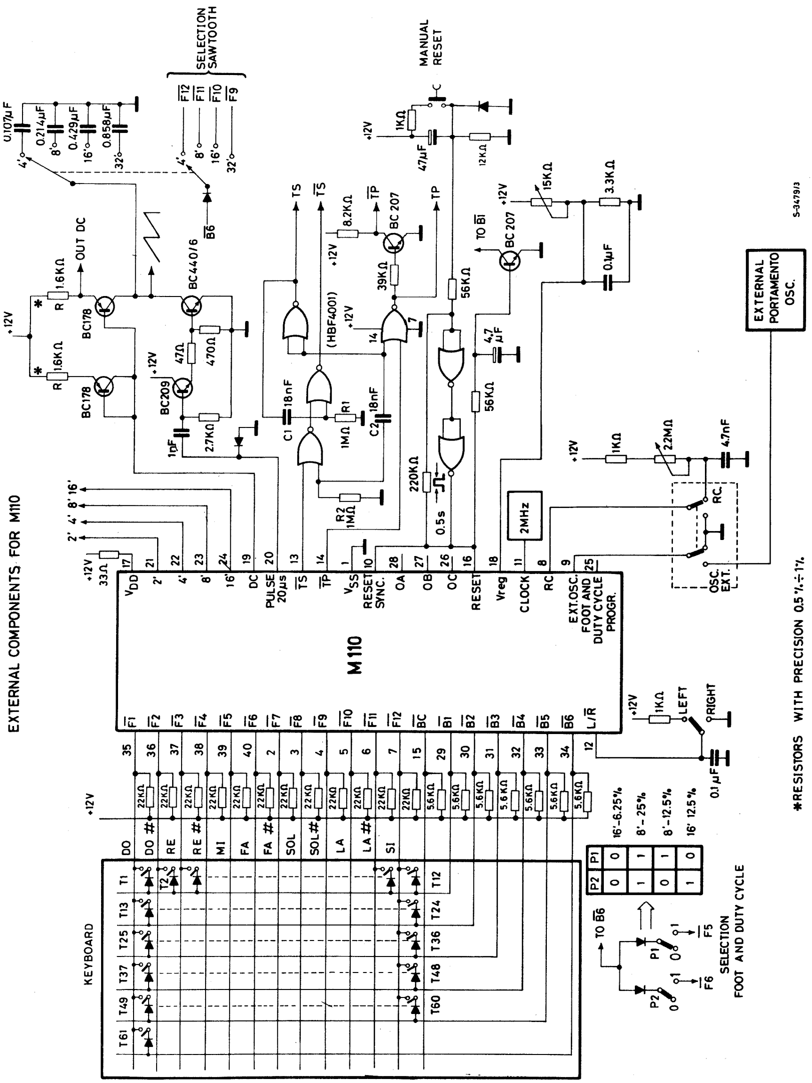
TIMING DIAGRAMS (KEYBOARD SCANNING)



*Signals inside the M110

INPUT CLOCK WAVEFORM (pin 11)





EXTERNAL COMPONENTS FOR M110

MOS INTEGRATED CIRCUIT

M 120

PRELIMINARY DATA

1024 BIT - NON VOLATILE RANDOM ACCESS MEMORY (NV-RAM)

- 256 x 4 ORGANIZATION
- OPTIMUM DATA RETENTION: ONE ORDER OF MAGNITUDE GREATER THAN MNOS DEVICES
- MORE THAN 10^4 MODIFY OPERATIONS PER BIT
- THREE VERSIONS WITH DIFFERENT READ AND MODIFY ACCESS TIMES: M120-2:450 ns -- M120 : 700 ns -- M120-4 : 950 ns
- INTERNAL WORD MODIFY TIME LESS THAN 100 msec
- "MODIFY END" OUTPUT LINE
- TTL COMPATIBLE: EASY CONNECTION TO ANY MICROPROCESSOR
- COMMON DATA INPUTS AND OUPUTS
- ON CHIP LATCHES FOR ADDRESSES AND DATA
- POWER SUPPLIES V_{DD}= 12V ± 10%
  V_{PP} = 25V ± 5%
- STANDARD 18-PIN DUAL-IN-LINE PACKAGE

The M120 is a new Non Volatile Random Access Memory (NV-RAM). Contents of every word (256 x 4 available on-chip) can be erased and written electrically and data is retained without power supply for 100 years (calculated from test results). SGS-ATES proprietary n-channel, Si-gate, double Polysilicon MOS Technology insures maximum reliability and data retention and allows any number of read operations and more than 10.000 modify cycles per bit. Thanks to an internal circuitry taking care of the modify sequence, access times for both read and modify operations are short enough to allow use with most microprocessors without insertion of wait states. The M120 is available in three different versions. The slowest M120-4 in particular, with 950 ns access time, is intended for applications where the M120 is used in combination with a single chip microcomputer. In these applications all the signals are supplied by the microcomputer I/O ports, and the access time required is always in the range of microseconds. The M120 is available in a standard 18-pin dual-in-line plastic or ceramic package (frit-seal).

ABSOLUTE MAXIMUM RATINGS*

	Input or output voltages (except V_{DD} and V_{PP})	-0.5 to 15	V
V_{DD}	Supply voltage	-0.5 to 20	V
V_{PP}	Supply voltage	-0.5 to 28	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stresses rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

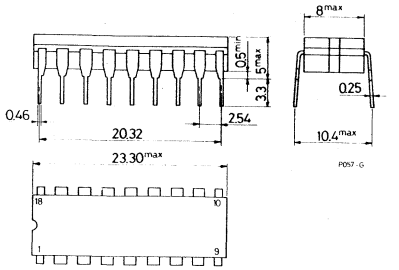
ORDERING NUMBERS:

M120F1	for dual in-line ceramic package (frit seal)
M120B1	for dual in-line plastic package
M120-2F1	for dual in-line ceramic package (frit seal)
M120-2B1	for dual in-line plastic package
M120-4F1	for dual in-line ceramic package (frit seal)
M120-4B1	for dual in-line plastic package

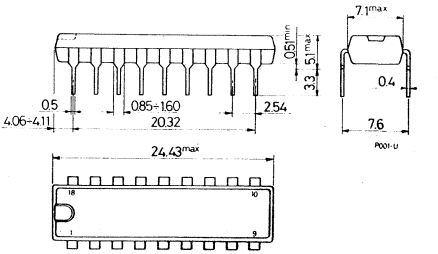
M 120

MECHANICAL DATA (dimensions in mm)

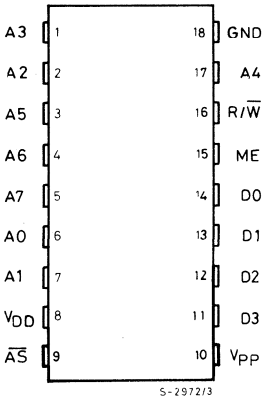
Dual in-line ceramic package, frit-seal



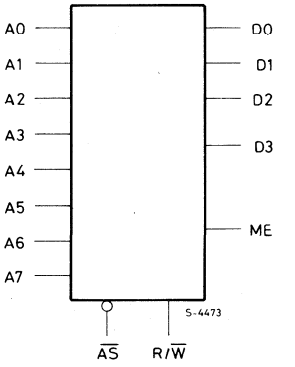
Dual in-line plastic package



PIN CONNECTIONS



LOGIC DIAGRAM



PIN NAMES

D0–D3	DATA INPUTS/OUTPUTS (OPEN DRAIN)
A0–A7	ADDRESS INPUTS
$\overline{AS}$	ADDRESS STROBE INPUT
R/$\overline{W}$	READ/WRITE INPUT
ME	MODIFY END OUTPUT (OPEN DRAIN)
V_{PP}	POWER (+25V)
V_{DD}	POWER (+12V)
GND	GROUND

DC AND OPERATING CHARACTERISTICS (T_{amb}= 0°C to 70°C, V_{DD}= +12V ± 10%, V_{PP}= +25V ± 5%)

Parameter		Test conditions	Values			Unit
			Min.	Typ.*	Max.	
I_{DD1}	V_{DD} supply current				30	mA
I_{PP1}	V_{PP} supply current				20	mA
I_{DD2}	Standby V_{DD} supply current	$\overline{AS}$ @ V_{IH}			20	mA
I_{PP2}	Standby V_{PP} supply current	$\overline{AS}$ @ V_{IH}			10	mA
V_{IH}	Input high voltage		2.4	5		V
V_{IL}	Input low voltage		-0.3	0	0.6	V
V_{OL}	Output low voltage	I_{OL}= 1.6 mA			0.4	V
I_{LI}	Input leakage current				10	μA
I_{LO}	Output leakage current				10	μA

* Typical values are at +25°C and nominal voltages.

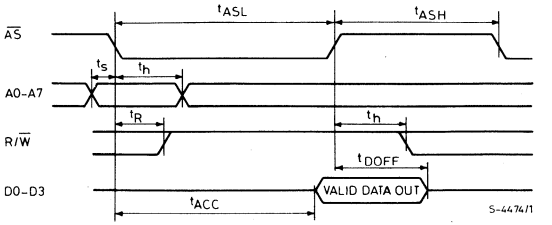
AC CHARACTERISTICS

Parameter		M 120-2		M 120		M 120-4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_s	Set-up time	50		50		100		ns
t_h	Hold time	150		150		250		ns
t_{ASL}	$\overline{AS}$ active time	450	100K	700	100K	950	100K	ns
t_{ASH}	$\overline{AS}$ inactive time	350		500		500		ns
t_R	$\overline{AS}\downarrow$ to R/$\overline{W}\uparrow$ (Read)		100		150		200	ns
t_{ACC}	Access time from $\overline{AS}\downarrow$		450		700		950	ns
t_{DOFF}	Data output turn-off delay		150		250		300	ns
t_M	Modify time (1) from R/$\overline{W}\uparrow$		100		100		100	ms
t_{WHE}	$\overline{AS}\downarrow$ to R/$\overline{W}\downarrow$ (Early write) (2) (3)		100		150		200	ns
t_{WE}	$\overline{AS}\downarrow$ to R/$\overline{W}\uparrow$ (Early Write)	450		700		950		ns
t_{MHE}	ME turn-on delay from R/$\overline{W}\downarrow$ (Early Write)		400		500		600	ns
t_{AS}	R/$\overline{W}\downarrow$ to $\overline{AS}\uparrow$ rising edge (Read/Write)	250		400		500		ns
t_{WH}	$\overline{AS}\downarrow$ to R/$\overline{W}\downarrow$ (Read/Write)	100		200		250		ns
t_{WL}	R/$\overline{W}$ Low time (Read/Write)	350	100K	500	100K	650	100K	ns
t_{DF}	Data Float from $\overline{AS}\downarrow$ (Read/Write)	150		250		300		ns
t_{MH}	ME turn-on delay from R/$\overline{W}\downarrow$ (Read/Write)		250		350		450	ns

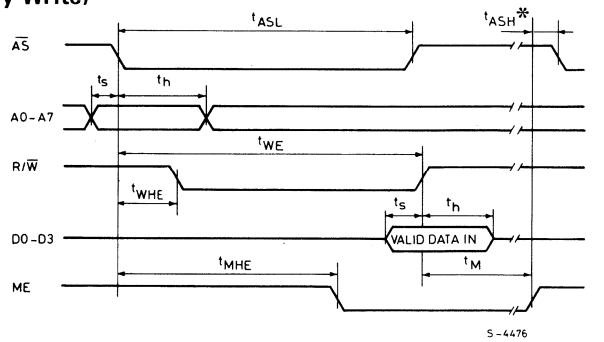
Notes:
1) $t_{M\ max}$ is 2 ms for the first 10 modify operations and increases to a maximum of 100 ms after 10^4 operations.
2) If $t_{WHE} \leqslant t_{WHE\ max}$ then D_{OUT} remains floating and there is no conflict between D_{OUT} and D_{IN}.
3) t_{WHE} can be < 0.

TIMING WAVEFORMS

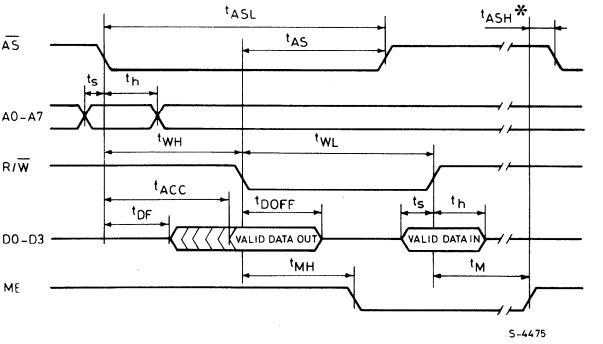
Read Cycle



Modify Cycle (Early Write)



Modify Cycle (Read/Write)



* The first falling edge of $\overline{AS}$ following the end of a modify cycle must occur at least t_{ASH} after the positive edge of ME.

DESCRIPTION OF OPERATION

M120 operation is controlled by the Address Strobe ($\overline{AS}$) control input (active low), which also performs the device selecting function.
The device is deselected (Stand-by Mode) by a high level on $\overline{AS}$ input.
The falling edge of $\overline{AS}$ latches Address lines (A0 ÷ A7) contents into the chip and starts both read and modify cycles.
If R/$\overline{W}$ remains high while $\overline{AS}$ is active a **Read Cycle** occurs. The contents of addressed memory location will be available on the Data lines (D0 ÷ D3) after an access time (t_{ACC}) from the leading edge of $\overline{AS}$.
The trailing edge of $\overline{AS}$ three-states Data lines after t_{DOFF} delay.
If R/$\overline{W}$ is or becomes low while $\overline{AS}$ is active a **Modify Cycle** starts.
Depending on timing relationships between $\overline{AS}$ and R/$\overline{W}$ leading edges, there are two possible modify sequences.
If R/$\overline{W}$ falling edge occurs either before or a maximum of t_{WHE} after $\overline{AS}$ falling edge, an **Early Write** Modify Cycle proceeds.
All timing relationships are related to $\overline{AS}$ falling edge and Data lines are not driven by the M120 thus avoiding any possible bus contention in this mode.
If R/$\overline{W}$ falling edge occurs a minimum of t_{WH} after $\overline{AS}$ falling edge a **Read/Write** Modify Cycle procedes.
Most timing relationships are in this case related to R/$\overline{W}$ falling edge. Because until R/$\overline{W}$ becomes active, the M120 assumes a read cycle is in process, the device will output addressed location contents on Data lines according to t_{DF}, t_{ACC} and t_{WH} timing specifications.
This allows a read/write operation to be performed but might also generate some contention on data lines.
However if set-up time requirements are satisfied, the M120 will operate properly since it floats data lines before latching data input.

INTERNAL MODIFY OPERATION AND "ME" OUTPUT

At rising edge of R/$\overline{W}$ in a modify cycle the contents of data lines are latched and the internal modify cycle starts.
The ME output, which indicates Modify Cycle End, goes false (low) after a delay of either t_{MHE} from $\overline{AS}$ leading edge (Early Write Modify Cycle) or t_{MH} from R/$\overline{W}$ falling edge (Read/Write Modify Cycle).
As long as ME is false the device is internally disconnected from buses and control lines, data outputs are floating and no further external operation will be acknowledged by M120.
During internal modify cycle an on-chip circuitry performs a bit by bit comparison between "old" and "new" data word and according to this result writes, erases or leaves unchanged each single bit of the addressed location.
At modify completion (t_M) ME line becomes true again and M120 is again available for external access.

POWER-UP

In order to avoid a spurious modify cycle, care should be taken during the power up sequence to ensure that $\overline{AS}$ and R/$\overline{W}$ are at the non-active (high) level before V_{DD} and V_{PP} reach half their operating value.
The opposite sequence should be followed during the power-down.
Power-on and power-down sequences can start arbitrarily with either V_{DD} or V_{PP}.

QUAD 80-BIT STATIC SHIFT REGISTER

- SINGLE VOLTAGE SUPPLY: $V_{CC} = 5V \pm 5\%$
- DC to 3 MHz OPERATION GUARANTEED
- FULLY TTL COMPATIBLE
- FULLY DC OPERATION
- SINGLE LINE CLOCK
- PIN-FOR-PIN REPLACEMENT for MK 1007P-TMS 3409 - 2532 - 3347
- LOW POWER DISSIPATION: 250 mW (TYP.)
- INPUT GATE PROTECTION
- M142A IS A HIGH SPEED SELECTION

The M142 and M142A are quad 80-bit fully DC shift register constructed on a single chip using very low threshold N-channel silicon gate technology which allows high speed (3 MHz guaranteed) and fully TTL compatibility without using any external resistor.
Each of the four 80-bit registers has an independent input, output and recirculate control. The single clock line is common to all four registers.
Transferring data into the register is accomplished when the clock is high (logic "1") Shifting of data occurs when the clock goes low. Output data appears on the negative going edge of the clock.
When the recirculate line is high, data recirculates, while input is inhibited. When data is entered, the recirculate line is at logic "0".
Output data attain the same logic state that was shifted into the register 80 clocks prior. Available in 16-lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{CC}	Supply voltage	-0.5 to 7	V
V_i	Input voltage on any pin	-0.5 to 7	V
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

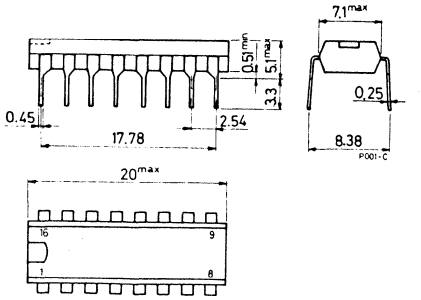
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS:

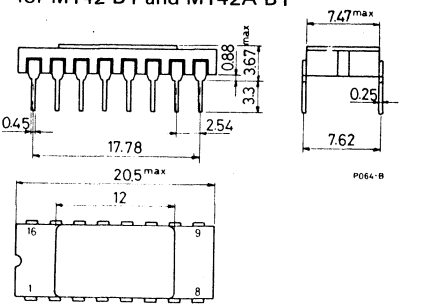
M142 B1 for dual in-line plastic package
M142 D1 for dual in-line ceramic package
M142A B1 for dual in-line plastic package
M142A D1 for dual in-line ceramic package

MECHANICAL DATA (dimensions in mm)

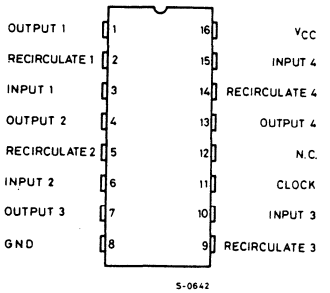
Dual in-line plastic package
for M142 D1 and 142A D1



Dual in-line ceramic package
for M142 B1 and M142A B1

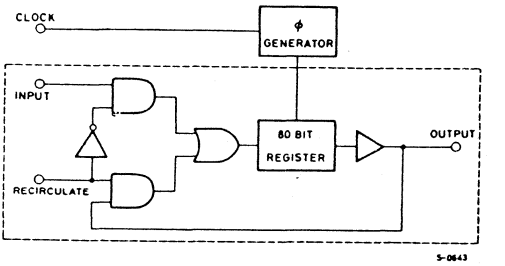


PIN CONNECTIONS



BLOCK DIAGRAM

(one of four shown)



TRUTH TABLE
(positive logic)

Recirculate	Input	Function
"0"	"0"	"0" is written
"0"	"1"	"1" is written
"1"	"0"	Recirculate
"1"	"1"	Recirculate

"0" = 0V, "1" = 5V

STATIC ELECTRICAL CHARACTERISTICS (V_{CC}= 5V ± 5%, T_{amb}= 0 to 70°C unless otherwise specified)

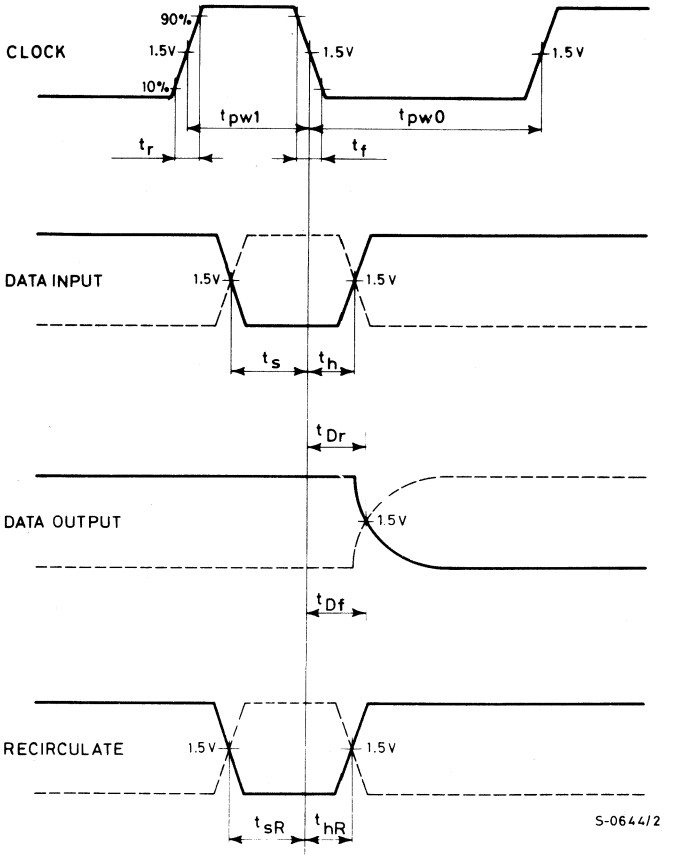
Parameter		Test conditions	Values**			Unit
			Min.	Typ.	Max.	
V_{IH}*	Input high voltage		2		V_{CC}	V
V_{IL}*	Input low voltage		-0.3		0.8	V
V_{OH}	Output high voltage	I_{OH}= -100 μA	2.4			V
V_{OL}	Output low voltage	I_{OL}= 1.6 mA			0.4	V
I_{LI}*	Input leakage current	$V_i = V_{CC}$			10	μA
I_{CC}	Supply current			48		mA

* These parameters apply to all inputs including clock.
** Typical values at T_{amb}= 25°C and V_{CC}= 5V.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{CC}= 5V ± 5%, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
f	Clock repetition rate					3	MHz
$t_{\phi\ pw1}$	Clock high pulse width			110			ns
$t_{\phi\ pw0}$	Clock low pulse width			220			ns
t_r, t_f	Clock rise and fall time					5	μs
t_{setup}	Setup time			100			ns
t_{hold}	Hold time			80			ns
t_{sR}	Recirculate setup time			100			ns
t_{hR}	Recirculate hold time			80			ns
t_{Dr}, t_{Df}	Delay time to rise and fall	TTL load C_L= 10 pF	for **M142** type for **M142A** type			230 160	ns ns
C_{iR}	Recirculate input capacitance	V_i = 0V	f = 1 MHz			8	pF
C_ϕ	Clock capacitance	V_ϕ= 0V	f = 1 MHz			12	pF

WAVEFORMS


CLOCK
90%
1.5V
10%
1.5V
1.5V
tpw1
tpw0
tr
tf
DATA INPUT
1.5V
1.5V
ts
th
tDr
DATA OUTPUT
1.5V
tDf
RECIRCULATE
1.5V
1.5V
tsR
thR
S-0644/2

16 KEY KEYBOARD ENCODER AND LATCH

- ANTIBOUNCE AND ANTINOISE CIRCUITRY
- INTERLOCK PREVENTS INCORRECT SELECTION
- OPERATES WITH SINGLE POLE PUSH-BUTTONS
- SELECTION OF PROGRAM 1 AT POWER ON
- MUTING OUTPUT AVAILABLE DURING PROGRAM CHANGES AND POWER SUPPLY SWITCHING
- STEP-BY-STEP PROGRAM CHANGE INPUT
- KEYBOARD LOCKING
- OUTPUTS DIRECTLY COMPATIBLE WITH M 193 (ELECTRONIC PROGRAM MEMORY), M 192 (7-SEGMENT DECODER DRIVER), H 770/1/2/3 (QUAD ANALOG SWITCHES)

The M 190 is a monolithic integrated circuit which automatically scans an up to 16 Key keyboard, generating continuous sequential pulses on X outputs and detecting key closure on Y inputs.
A key closure is retained as valid when the key remains closed for all the time corresponding to one scan pulse (i.e. when the bounce is over).
When it occurs an internal flip-flop is set but the key closure is accepted only if it is detected on a second scan cycle. At this point a 4 bit word corresponding to the key closed is internally latched and a pulse is available on the Muting output.
During the time this pulse lasts, no other key closure will be recognized. The new output code follows the Mute signal with a delay.
All the timing for the circuits is determined by the clock oscillator whose frequency is externally fixed by an RC network.
The M 190 also includes a "step-by-step" program change input that, when connected to V_{SS} (GND), advances by one the selected channel and a Lock which blocks the circuit on the last selected channel.
The circuit is produced in N-channel silicon gate technology and is available in a 18 pin dual in-line plastic package.

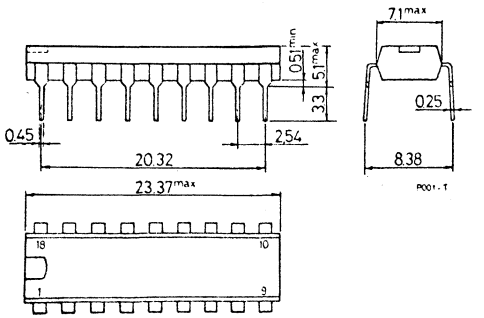
ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to 20	V
$V_{O(off)}$	Off state output voltage (pins 1-2-3-4-11)	20	V
I_O	Output current	|5|	mA
P_{tot}	Total package power dissipation	500	mW
T_{stg}	Storage temperature	-65 to 125	°C
T_{op}	Operating temperature	0 to 70	°C

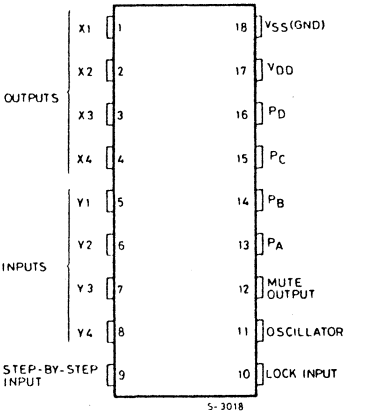
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
** All voltage are referred to V_{SS} pin voltage.

ORDERING NUMBER: M 190 B1

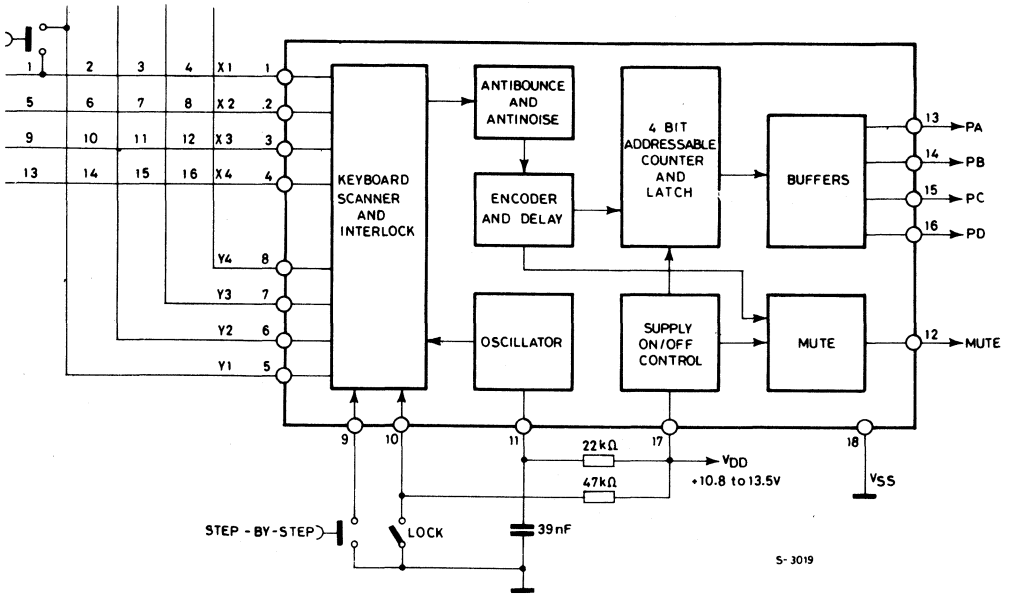
MECHANICAL DATA (dimensions in mm)



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	10.8 to 13.5	V
V_I	Input voltage	0 to 13.5	V
$V_{O(off)}$	Off state output voltage (pins 1-2--3-4-11)	max 13.5	V
I_O	Output current	max |2|	mA
T_{op}	Operating temperature	0 to 70	°C
R_t	Timing resistor	8 to 47	KΩ
C_t	Timing capacitor	1 to 330	nF

STATIC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Parameter		Test conditions	Values at 25°C			Unit
			Min.	Typ.	Max.	
V_{IH}	High level input voltage	pins 5, 6, 7, 8, 9, 10	3.5			V
V_{IL}	Low level input voltage	pins 5, 6, 7, 8, 9, 10			0.8	V
I_{IH}	High level input current	V_{DD}= 13.5V, V_{IH}= 13.5V pins 5, 6, 7, 8, 9, 10			10	μA
I_{IL}	Low level input current	V_{DD}= 13.5V, V_{IL}= 0.8V pins 5, 6, 7, 8, 9, 10	0.1		0.8	mA
V_{OH}	High level output voltage	V_{DD}= 10.8V I_{OH}= -1 mA, pin 12	2.4			V
		V_{DD}= 10.8V I_{OH}= -1 mA, pins 13. 14, 15, 16	4			
V_{OL}	Low level output voltage	V_{DD}= 10.8V I_{OL}= 0.8 mA pins 1, 2, 3, 4, 11			0.4	V
		V_{DD}= 10.8V I_{OL}= 2 mA, pins 13, 14, 15, 16			0.4	
$I_{O(off)}$	Output leakage current	V_{DD}= $V_{O(off)}$= 13.5V, pins 1, 2, 3, 4, 11			20	μA
I_{DD}	Supply current	V_{DD}= 13.5V (all inputs and outputs open)			18	mA

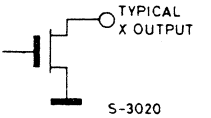
TRUTH TABLE

Key	Connection	Output code (positive logic)			
		PA	PB	PC	PD
1	$X_1 - Y_1$	L	L	L	L
2	$X_1 - Y_2$	H	L	L	L
3	$X_1 - Y_3$	L	H	L	L
4	$X_1 - Y_4$	H	H	L	L
5	$X_2 - Y_1$	L	L	H	L
6	$X_2 - Y_2$	H	L	H	L
7	$X_2 - Y_3$	L	H	H	L
8	$X_2 - Y_4$	H	H	H	L
9	$X_3 - Y_1$	L	L	L	H
10	$X_3 - Y_2$	H	L	L	H
11	$X_3 - Y_3$	L	H	L	H
12	$X_3 - Y_4$	H	H	L	H
13	$X_4 - Y_1$	L	L	H	H
14	$X_4 - Y_2$	H	L	H	H
15	$X_4 - Y_3$	L	H	H	H
16	$X_4 - Y_4$	H	H	H	H

DESCRIPTION

Pins 1, 2, 3, 4 - X_1, X_2, X_3, X_4 outputs

The internal open drain transistors on these outputs are sequentially switched on.

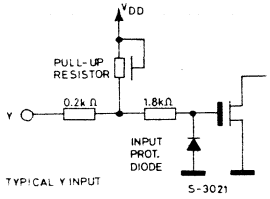


Pins 5, 6, 7, 8 - Y_1, Y_2, Y_3, Y_4 inputs

These inputs correspond to the columns of the keyboard matrix. When a key is pushed, one of the X output signal is present on one of the 4 rows, putting a low level on the Y input.
An interlock circuit rejects more than one key pressed at the same time.
To increase the noise immunity of the system and to avoid bouncing problems, the key closure is considered valid only when it is present for all the time corresponding to the scan pulse. With this system spurious noise signals are also rejected.
Another increase in the noise immunity is given by detecting key closure over two consecutive scanning cycles.

DESCRIPTION (continued)

After the key bounce time, the acceptance time of a command is between 35T and 63T, where T is the period of the clock pulse.
When any input is open it is pulled-up to logic H by an integrated MOS load of about 50 KΩ and protected by a diode.



Pin 9 - Step-by-step program change

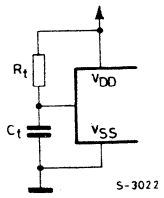
This input advances by one the previously selected channel every time ti is connedted to ground.
This input can be considered as a 17th key and follows all the rules of command acceptance time and partially of interlock.
The unput is pulled-up to logic H by an integrated resistor of about 50 KΩ ; if the input is not used, it should be connected to V_{DD}.

Pin 10 - Lock

If this input is connected to V_{SS} (GND) the circuit is locked on the selected channel.
If the input is not used, it must be connected to V_{DD}.

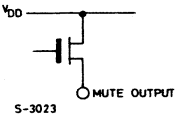
Pin 11 - RC network (clock oscillator input)

An internal clock provides all the timing for the circuits.
The frequency of the clock oscillator is controlled by two external components, resistor R_t and capacitor C_t.
The period of the clock pulse is approximately given by $T = R_tC_t$.
The oscillator works in the following way: assuming the capacitor C_t is discharged, the resistor R_t charges the capacitor till an internal threshold is reached. At this point the capacitor is discharged by an internal transistor.
Afterwards the internal transistor is switched off and the cycle can restart.
With R_t= 22 KΩ and C_t= 39 nF a clock frequency of about 800 Hz is obtained, corresponding to a scan cycle of the keyboard of about 40 ms.
In these conditions the mute signal will be present for about 100 ms before the program changing and will last 300 ms.

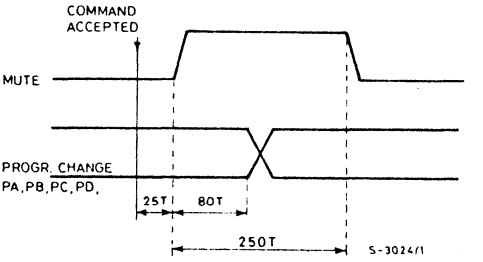


Pin 12 - Mute

The mute signal is available as a high level output (source follower transistor).
It is present during power ON/OFF and program changes.



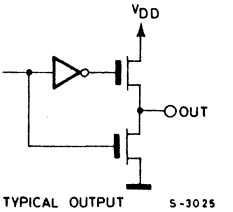
When a command is given the Mute signal and the program information are available in the following way:



The Mute signal is not available when the same program is selected again.

Pins 13, 14, 15, 16 - PA, PB, PC, PD outputs

These static outputs select the program according to the truth table.
They interface directly with the inputs of M 193 (Electronic Program Memory), M 192 (7 segment Decoder/Driver), H 770/1/2/3 (Quad Analog Switches).
The program 1 is internally selected at power ON.



MOS INTEGRATED CIRCUIT

M 192

4-BIT BINARY 7-SEGMENT DECODER DRIVER

- 4-BIT BINARY CODE INPUT GENERATES 1 TO 16 NUMBERS ON OUTPUT
- DIRECT DRIVING OF 1 AND 1/2 DIGIT 7-SEGMENT (COMMON CATHODE) LED DISPLAY
- WIDE SUPPLY VOLTAGE RANGE
- TTL COMPATIBLE INPUTS
- SMALL QUIESCENT SUPPLY CURRENT
- SPECIFICALLY DESIGNED FOR TV OR RADIO APPLICATIONS

The M 192 is a monolithic integrated circuit which direct drives a 1 and 1/2 digit 7-segment LED (common cathode) display to present the numbers 1 to 16. The inputs accept a 4-bit binary code having TTL levels. This device is especially designed to show the program number in TV or radio sets in conjunction with M 190 keyboard encoder, M 1130 ultrasonic remote control receiver, M 193 electronic program memory or H 770/1/2/3 analog switches. All outputs are designed to supply and sink current, except the additional "r" output (pin 1) which is designed for a brightness control in a current generator configurations. The circuit is produced in COS/MOS technology and is supplied in a 16-pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to 16.5	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
V_O	Output voltage (pin 1)	V_{DD} +0.5	V
I_{OH}	Output source current	-25	mA
I_{OL}	Output sink current (except pin 1)	10	mA
P_{tot}	Total package power dissipation	400	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

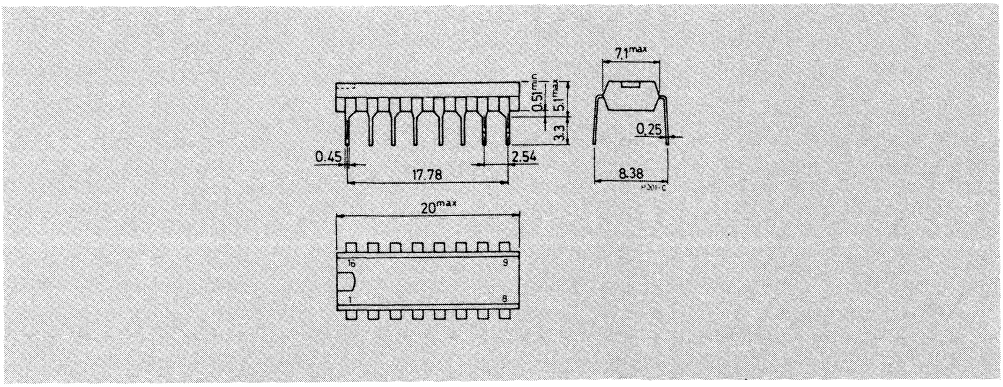
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

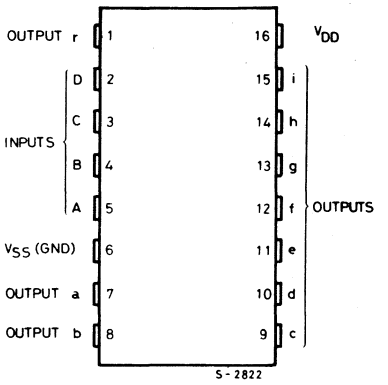
ORDERING NUMBER: M 192 B1

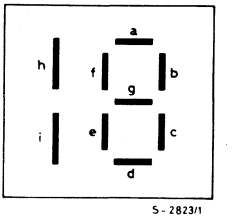
MECHANICAL DATA

Dimensions in mm



PIN CONNECTIONS

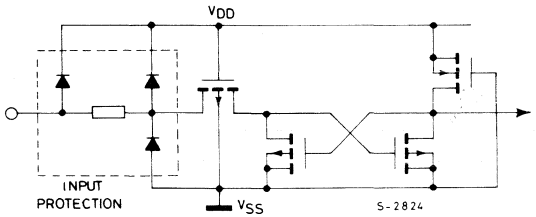




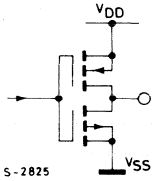
TRUTH TABLE

INPUTS				Number displayed	OUTPUTS									
A	B	C	D		a	b	c	d	e	f	g	h	i	r
L	L	L	L	1	L	H	H	L	L	L	L	L	L	H
H	L	L	L	2	H	H	L	H	H	L	H	L	L	H
L	H	L	L	3	H	H	H	H	L	L	H	L	L	H
H	H	L	L	4	L	H	H	L	L	H	H	L	L	H
L	L	H	L	5	H	L	H	H	L	H	H	L	L	H
H	L	H	L	6	H	L	H	H	H	H	H	L	L	H
L	H	H	L	7	H	H	H	L	L	L	L	L	L	H
H	H	H	L	8	H	H	H	H	H	H	H	L	L	H
L	L	L	H	9	H	H	H	H	L	H	H	L	L	H
H	L	L	H	10	H	H	H	H	H	H	L	H	H	H
L	H	L	H	11	L	H	H	L	L	L	L	H	H	H
H	H	L	H	12	H	H	L	H	H	L	H	H	H	H
L	L	H	H	13	H	H	H	H	L	L	H	H	H	H
H	L	H	H	14	L	H	H	L	L	H	H	H	H	H
L	H	H	H	15	H	L	H	H	L	H	H	H	H	H
H	H	H	H	16	H	L	H	H	H	H	H	H	H	H

INPUT CONFIGURATION



OUTPUT CONFIGURATION



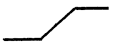
Note: pin 1 has not the pull down N-channel transistor.

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	10.8 to 15	V
V_I	Input voltage	0 to V_{DD}	V
V_O	Output voltage (pin 1)	V_{DD}	V
I_{OH}	Output source current	max -10	mA
I_{OL}	Output sink current	max 0.5	mA
T_{op}	Operating temperature	0 to 70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

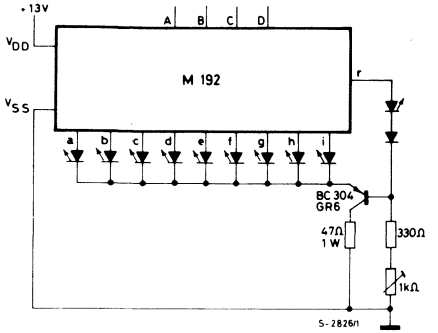
typical values are at T_{amb} = 25°C unless otherwise specified

Parameter		Test conditions	Values Min.	Values Typ.	Values Max.	Unit
V_{IH}	High level input voltage		3.5		V_{DD}	V
V_{IL}	Low level input voltage		0		0.8	V
I_{IH}	High level input current	V_{DD}= 15V V_{IH}= 15V			10	μA
I_{T+}	Input current at positive threshold	V_{DD}= 15V 			200	μA
V_{OH}	High level output voltage	I_{OH}= -10 mA V_{DD}= 10.8V V_{DD}= 13V V_{DD}= 13V, T_{amb}= 70°C V_{DD}= 15V	V_{DD} -3	V_{DD}-3 V_{DD}-2 V_{DD}-2.5 V_{DD}-1.5		V V V V
V_{OL}	Low level output voltage (except pin 1)	V_{DD}= 13V I_{OL}= 0.5 mA		1	1.5	V
I_{DD}	Supply current Input to V_{DD} Outputs open	V_{DD}= 15V		2	2,4	mA

APPLICATION INFORMATION

Fig. 1 - Light emitting diode readout

a - Current generator configuration



b - Standard configuration

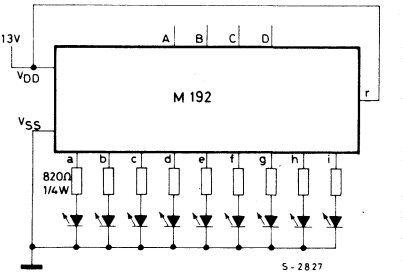


Fig. 2 - Liquid crystal readout

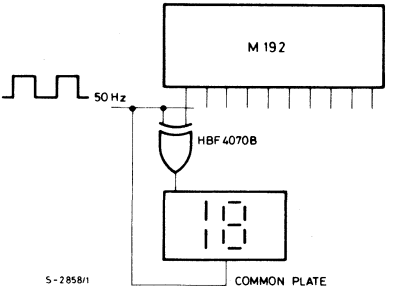


Fig. 3 - Fluorescent readout

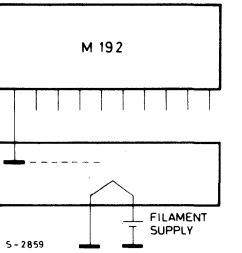


Fig. 4 - Incandescent redout

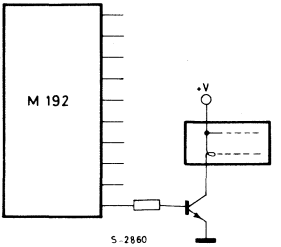
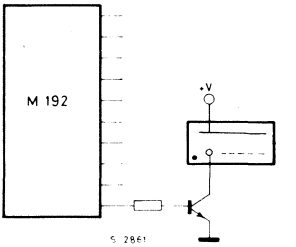


Fig. 5 - Gas discarge readout



TYPICAL APPLICATIONS (continued)

Program display with stand-by indication

This application is useful in a remote controlled set. The stand-by condition of the set, i.e. when only the remote control is supplied, is shown by two dots.

The program display number is controlled by the same output of the remote control receiver as that which drives the mains relay.

Fig. 6

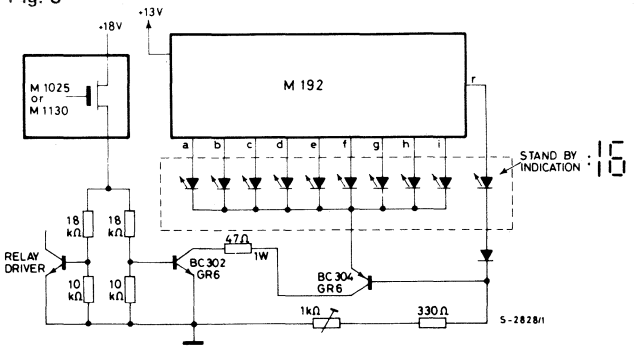
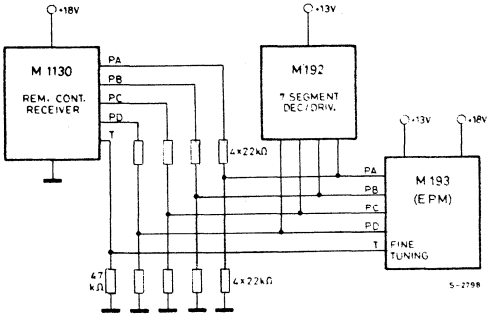
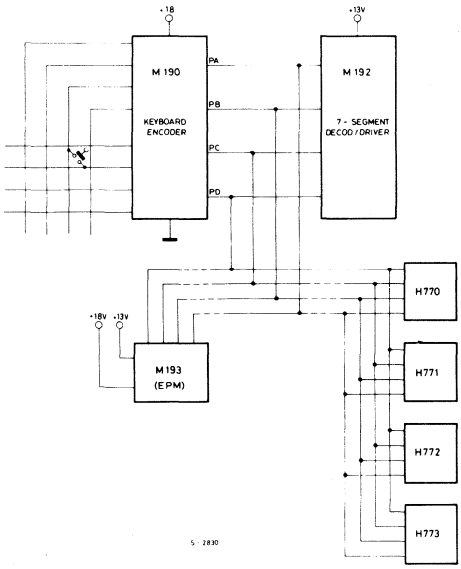


Fig. 7 - M 192 interfacing

a



b



EPM 16-ELECTRONIC PROGRAM MEMORY (16 STATIONS)

- ONE CHIP SOLUTION INCLUDING CONTROL AND NON VOLAT. MEMORY FOR 16 PROGR.
- 10 YEARS MEMORY RETENTION
- UNLIMITED NUMBERS OF READ CYCLES
- AUTOMATIC AND MANUAL STATION SEARCH
- EXTERNALLY ADJUSTABLE SEARCH SPEED
- FINE TUNING IN 8 STEPS, STORABLE FOR EACH PROGRAM SEPARATELY
- MUTE OUTPUT
- 4.43 MHz QUARTZ REFERENCE FREQUENCY

The M193 is a monolithic integrated circuit constructed in N-channel silicon gate technology, designed to control digitally via a D/A converter, with a resolution of 8192 steps, a TV or Radio varicap tuner. A 17 bit x 16 words NVRAM is also integrated in the chip. Each memory word contains information for 1 program, i.e. band (2 bit), tuning voltage (12 bit) and fine tuning offset (3 bit). The circuit is able to operate either in automatic or manual search. The search speed is externally controlled by a simple RC network. In the automatic mode the M193 works in conjunction with the TDA 4431, which provides TV station recognition and converts the AFC-S-curve into a digital command. This command controls the 13 bit up/down counter in the M193, whose position determines the tuning voltage. A mute output is provided to avoid noise on the audio during automatic search, program change or when the supply voltage is switched on/off. The circuit accepts standard program selection on 4 bus lines. 7-segment program display is possible using the M192 circuit connected at the same lines. A serial information output is provided to display on the screen, via the M191 integrated circuit, the varicap voltage in the form of a linear tuning bar and the band. The M193 is available in a 28 lead dual in-line plastic package. Three different types are available which differ as specified below.

M193A - The automatic search is implemented with two commands which provide to scan the bands I + UHF and III + S respectively.

M193C - The search, either automatic or manual, is done only in the selected band. The band can be changed with a separate step-by-step command.

M193D - Same search function characteristics of the C type. The only difference consists in the threshold of discrimination of pulses applied at pin 4 (fine tuning from remote control). This version interfaces with the "T" output of the SAA 1251 remote control receiver.

ABSOLUTE MAXIMUM RATINGS*

V_{DD1}, V_{DD2} **	Supply voltages	-0.3 to 20	V
V_{PP}	Memory supply voltage (pin 9)	-0.3 to 31	V
V_I	Input voltage	-0.3 to 20	V
$V_{O\,(off)}$	Off-state output voltage (except pin 14)	20	V
	(pin 14)	31	V
I_{OL}	Output current (except pins 15-19)	5	mA
	(pins 15-19)	15	mA
I_{OH}	Output current (pin 27)	-5	mA
P_{tot}	Total package power dissipation	1	W
T_{stg}	Storage temperature	-25 to 125	°C
T_{op}	Operating temperature	0 to 70	°C

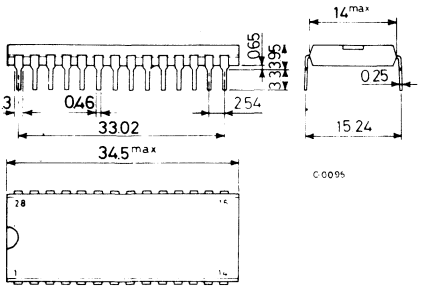
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

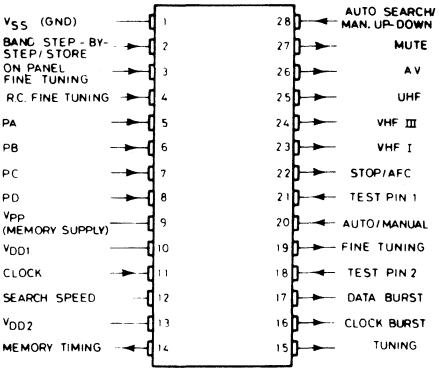
ORDERING NUMBERS: M193A B1
M193C B1
M193D B1

M 193A
M 193C
M 193D

MECHANICAL DATA (dimensions in mm)



PIN CONNECTIONS



NOTE : TEST PINS must be connected to V_{SS} (GND)

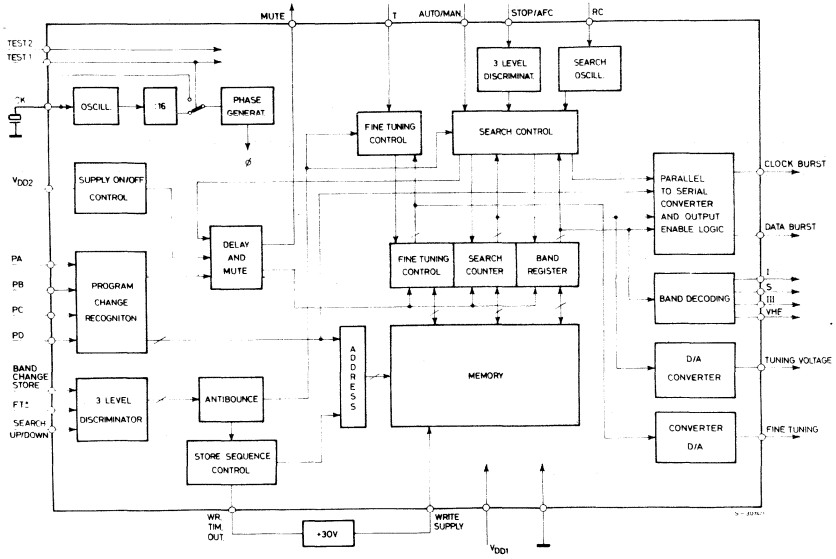
S-3215/1

RECOMMENDED OPERATING CONDITIONS

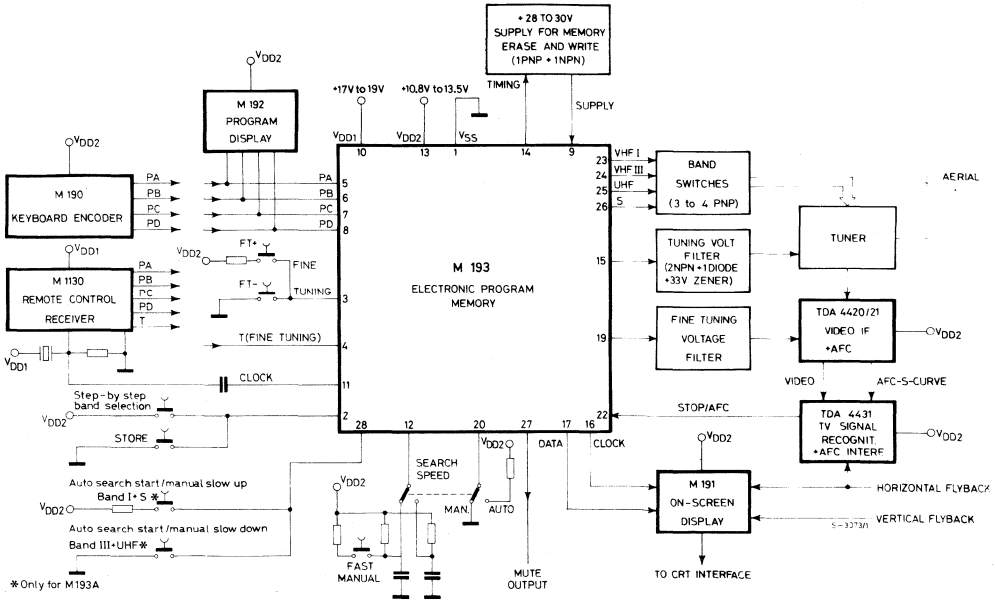
V_{DD1}	Supply voltage		17 to 19	V
V_{DD2}	Supply voltage		10.8 to 13.5	V
V_{PP}	Memory supply voltage (pin 9)		28 to 30	V
V_I	Input voltage		0 to 19	V
$V_{O(off)}$	Off-state output voltage (except pin 14)		max. 19	V
	Off-state output voltage (pin 14)		max. 30	V
I_{OL}	Output current (except 15--19)		max. 2.5	mA
	(pins 15-19)		max. 10	mA
I_{OH}	Output current (pin 27)		max. -2.5	mA
t_{pd}	Delay between memory timing and memory supply pulses		max. 5	μs
f	Clock frequency		4.4	MHz
R_s	Serial resistance of the quartz		max. 50	Ω
C_d	Dynamic capacitance of the quartz		max. 20	fF
C_p	Total parallel capacitance of the quartz		max. 8	pF
R_p	Total parallel resistance of the quartz		min. 10	MΩ
t_{w1}	Fine tuning + pulse width (pin 4)	M193A, C	$>$ 1.8	ms
		M193D	$>$ 120	μs
t_{w2}	Fine tuning - pulse width (pin 4)	M193A, C	$<$ 1.7	ms
		M193D	$<$ 80	μs
T_{op}	Operating temperature		0 to 70	°C
R_{12}	Search speed resistance (pin 12)		18 to 330	KΩ
C_{12}	Search speed capacitor (pin 12)		max. 100	nF

Notes: 1) The oscillator of the M193 cannot be used to drive external circuits.
2) See the "General information" at the end of this data as far as the power-on supply sequence is concerned.

BLOCK DIAGRAM



EPM SYSTEM CONFIGURATION



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at T_{amb}= 25°C, V_{DD1}= 18V, V_{DD2}= 12V unless otherwise specified

Parameter		Pins	Test conditions			Values			Unit
						Min.	Typ.	Max.	
V_{IL}	Low level input voltage	4-5-6-7-8						0.8	V
		2-3-20-22-28						1.3	
V_{IH}	High level input voltage	4-5-6-7-8				3.5			V
		2-3-28-20				V_{DD2}-2			
		22				V_{DD2}-1			
V_{IM}	Middle level input voltage	22	V_{DD2}= 10.8V			4,5		7.5	V
			V_{DD2}= 13.5V			5		9	
V_{OL}	Low level output voltage	23-24-25-26	V_{DD2}= 10.8V	I_{OL}= 1 mA				3	V
		15-19	V_{DD2}= 10.8V	I_{OL}= 10 mA				1	
		16-17	V_{DD2}= 10.8V	I_{OL}= 1 mA				0.5	
		14	V_{DD1}= 17V V_{DD2}= 10.8V	I_{OL}= 2.5 mA				8	
V_{OH}	High level output voltage	27	V_{DD2}= 10.8V	I_{OH}= -1 mA		2.4			V
$I_{O(off)}$	Output leakage current	27	V_{DD2}= 13.5V	$V_{O(off)}$= V_{SS}				-50	µA
		23-24-25-26	V_{DD2}= 13.5V	$V_{O(off)}$= 19V				100	
		15-16-17-19	V_{DD2}= 13.5V $V_{O(off)}$= 13.5V					50	
		14	V_{DD1}= 19V $V_{O(off)}$= 30V	V_{DD2}= 13.5V				100	
I_I	Input current	4-5-6-7-8-22	V_I = 0 to 19V					|25|	µA
I_{DD1}	Supply current	10	V_{DD1}= 19V					3	mA
I_{DD2}	Supply current	13	V_{DD2}= 13.5V				32	45	mA
I_{PP}	Memory supply current	9	V_I= 30V	write	peak			65	mA
					average			16	
				erase	peak			1	
					average			0.5	
R_I	Input resistance	2-3-28	See Fig. 1a				0.5		MΩ

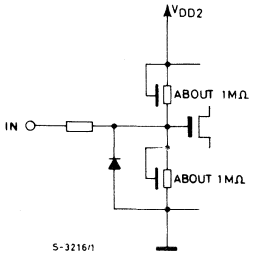
DYNAMIC ELECTRICAL CHARACTERISTICS (f_{clock} = 4.43 MHz)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
f_o	Fine tuning output repetition rate	Pin 19 (see also fig. 9)		17305		Hz
D	Fine tuning output duty cycle		1/8		8/8	
t_{w3}	Width of erase pulses	Pin 14		115		µs
T_3	Period of erase pulses	See also fig. 3 and 6		231		µs
t_3	Total time for one erase cycle (about 500 pulses)			115		ms
t_{w4}	Width of write pulses	Pin 14		115		µs
T_4	Period of,write pulses	See also fig. 2 and 5		462		µs
t_4	Total time for one write cycle about 950 pulses)			440		ms
t_{w5}	Width of clock pulses	Pin 16		1.3		µs
T_5	Period of data and clock pulses	Pin 17 See also fig. 8		3.6		µs
t_5	Total time for one display burst (15 pulses)			54		µs
t_6	Burst repetition time			3.69		ms
t_7	Acceptance time of the commands	Pins 2-3-28		31		ms
t_8	Acceptance time of the commands	Pin 20		3.6		µs

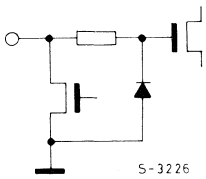
Input and output configurations
All outputs (except the Mute one) have open drain configuration.
The Mute output has a source follower.
Inputs have the following configurations:

Fig. 1

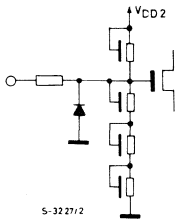
a) Pins 2, 3, 28



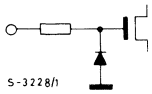
b) Search speed (pin 12)



c) Clock input (pin 11)



d) Other inputs (pin 4-5-6-7-8-12-20-21-22)



DESCRIPTION

The circuit description will be made following both pin sequence and pin function.

Pin 1 - V_{SS} (GND)

The substrate of the integrated circuit is connected to this pin. It is the reference point for all voltage parameters of the device and must be connected to the lowest potential of the supply voltage, normally ground.

Pin 2 - Store/sequential band change input

If this input pin is briefly connected to V_{SS} the 12 bits of the digitized tuning voltage, the 2 bits for band selection and the 3 bits of fine tuning information are stored.
The command is disabled during search and the execution of the store cycle.
The store cycle consists of two operations: at first the old word is cancelled and afterwards the new content is written.
If this input pin is briefly connected to V_{DD}, the selected band output changes in the sequence written below, to obtain a step-by-step band selection.

VHF III
UHF
VHF I
S
VHF III and so on

Pin 3 - Fine tuning +/— (on panel)

This input accepts the Fine tuning +/— commands given from the panel.
The commands are accepted according to the following rules:

Input levels	Command
M (input floating)	No command
H	FT +
L	FT —

Each command corresponds to one step change; to have more changes the key must be released and the command repeated.

Pin 4 - T input (fine tuning +/— from remote control)

The Fine tuning +/— commands given from Remote control are applied to this input in the form of a series of positive pulses. The threshold of discrimination of the pulses is different for the M193A, C and the M193D.

Type	t_{w1} (FT +)	t_{w2} (FT -)
M193A and C	> 1.8 ms	< 1.7 ms
M193D	> 120 μs	< 80 μs

The M193A and C are compatible with the M1130 remote control receiver.
The M193D interfaces with either the M1130 and the SAA 1251 receivers.
When the Fine tuning command is given, the duty cycle of the output of pin 19 (Fine tuning output) is changed at the rate of one step every 0.56 sec.
If the pulses are present for less than 0.56 sec. step-by-step operation can be obtained.
If this input is not used it must be connected to V_{SS} (GND).

Pins 5-6-7-8 - Program inputs

This 4-line bus selects the program according to the truth table given below:

Program	PA	PB	PC	PD
1	L	L	L	L
2	H	L	L	L
3	L	H	L	L
4	H	H	L	L
5	L	L	H	L
6	H	L	H	L
7	L	H	H	L
8	H	H	H	L
9	L	L	L	H
10	H	L	L	H
11	L	H	L	H
12	H	H	L	H
13	L	L	H	H
14	H	L	H	H
15	L	H	H	H
16	H	H	H	H

Pin 9 - V_{PP} - Memory supply

A series of pulses is applied to this pin during the store cycle. The timing of these pulses is given by the output of pin 14 and it is different during erase and write cycle as shown in fig. 2 and 3.
During a store cycle the old word is at first cancelled and the new one is written afterwards.

Fig. 2 - Memory Erase supply

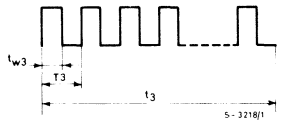
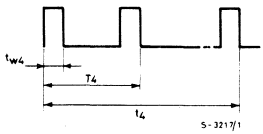


Fig. 3 - Memory Write supply



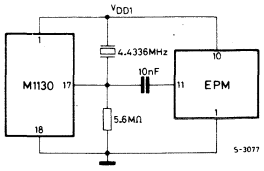
Pin 10 - V_{DD1}

This pin has to be connected to a power supply with the characteristics shown in the recommended operating conditions.

Pin 11 - Clock input

When the device is used alone the internal oscillator operates with a 4.43 MHz crystal connected between pin 11 and ground.
It can also operate with a single crystal together with M1130 as shown in fig. 4.
It is not suggested to use the oscillator of the M193 to drive external circuits.

Fig. 4



Pin 12 - Search speed

An external RC network is connected to this pin in order to set the frequency of the internal oscillator which, in turn, sets the scan speed during Search mode.
The scan speed can be adjusted over a wide range.
The relationship of search speeds between UHF, VHF and S is a follows:

Automatic:

FAST UP VHF = the frequency externally fixed
FAST UP UHF = S = 1/2 FAST UP VHF
MEDIUM DOWN VHF = 1/4 FAST UP VHF
MEDIUM DOWN UHF = S = 1/4 FAST UP UHF (1/8 FAST UP VHF)
SLOW UP VHF = UHF = S = 67.7 Hz
SLOW DOWN VHF = UHF = S = 8.4 Hz

Manual: UP or DOWN UHF = S = 1/2 UP of DOWN VHF

The manual Fast up or down speed is obtained by changing the frequency of the oscillator. The maximum capacitance which should be connected to this pin is 100 nF.

Pin 13 - V_{DD2}

This pin has to be connected to a power supply with the characteristics indicated in the recommended operating conditions.

Pin 14 - Memory write timing output

This output gives the timing for the pulses to be applied on pin 9 during the store cycle. The output consists of an open drain transistor.
The waveforms are shown in fig. 5 and 6, and are different during erase and write cycle, as already described for pin 9.

Fig. 5 - Memory Erase Current

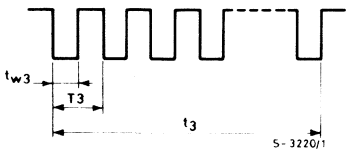
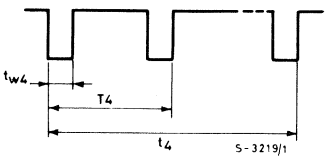


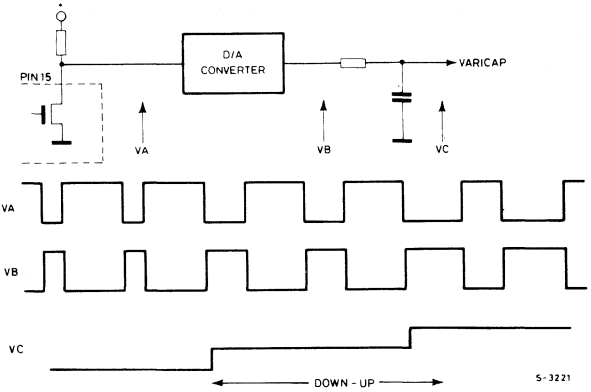
Fig. 6 - Memory Write Current



Pin 15 - Digitized tuning voltage output

The output consists of a variable frequency/variable width pulse train which, after filtering, provides the tuning voltage to the varicaps.
This signal carries 13 bits of information (only 12 bits however are stored in the memory).
The output circuit consists of an open drain transistor which offers a low impedance to ground when in the on state.
The output waveforms are shown in fig. 7.

Fig. 7



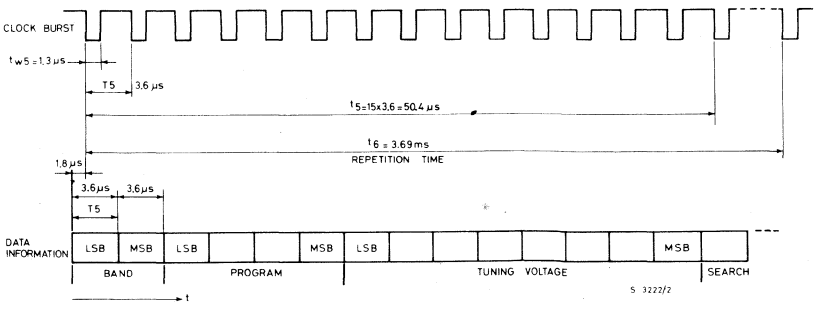
Pin 16 - Clock output for external display

A burst containing 15 clock pulses is available on this pin. These clock pulses are synchronized with Data Information as described in fig. 8.

Pin 17 - Data output for external display

A 15 bit burst is available on this pin.
In contains the 8 most significant bits of the digitized tuning voltage, 2 bits for band information, 4 bits for program information and 1 bit which indicates whether the system is in the Search mode (both in automatic and manual). This data is in complementary form (see fig. 8).
These two outputs (pins 16 and 17) work in connection with the M191 (On screen tuning bar display).
When the burst is not transmitted, the output transistor is in the off position.

Fig. 8



Pins 18 - 21 - Test pins

These pins must be connected to V_{SS} (GND).

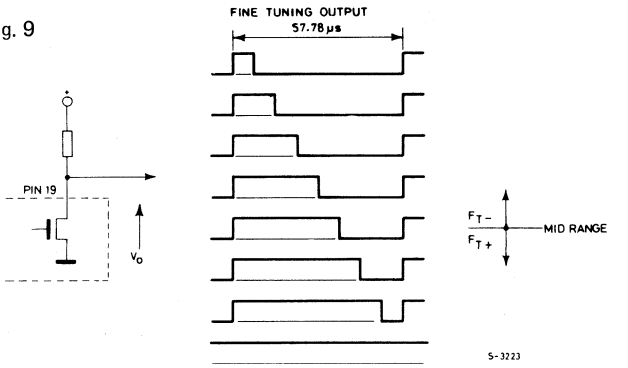
Pin 19 - Fine tuning output

Fine tuning information is available on this pin in the form of a square wave having a frequency of 17305 Hz and duty cycle variable in 8 positions as indicated in fig. 9.
The voltage generated after filtering is fed to the AFC loop and detunes the receiver by a small Δf while maintaining the action of the AFC.
The Fine tuning function operates as follows:

- during the search the output is set at mid-range (see fig. 9).
- when the search has been completed it is possible to operate on the Fine tuning +/— commands (pin 3 for Remote control operation or pin 4 for panel operation). The Store command memorizes this information together with the 12 bit tuning voltage and 2 bit band information
- when a memorized program is recalled it is still possible to act on the Fine tuning commands.

Any change in Fine tuning is only memorized by the Store command.

Fig. 9



Pin 20 - Automatic/manual selection

This pin is used to change the Search mode. When it is connected to V_{DD} the system operates in Automatic mode; when it is at V_{SS} (GND) the system works manually. The change Auto-manual or viceversa can be made at every time without precluding the right operation of the system.

Pin 22 - Stop/afc input

This pin is used only in automatic search mode.
When the EPM is in manual operation this pin is internally disabled.
The Stop/afc is also internally disabled during any program change for the time the Mute signal lasts. This input can have three different levels: high (H), middle (M), low (L). The middle level, unlike the other three level inputs of the circuit, is not internally generated and has to be externally determined according to the recommended operating conditions. If this input is not used it has to be connected to V_{SS} (GND) or to V_{DD2}.

The input has two different functions depending on whether the system is in the search or in normal operation (AFC control).

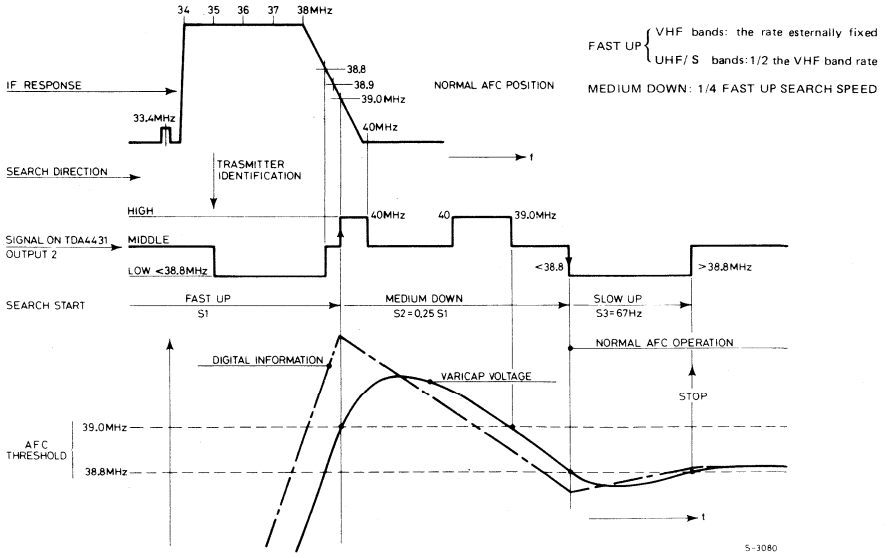
A) **Search mode:** after depressing the Search start key, the transitions and levels of the signals coming from the TDA 4431, applied to this pin, control the search function and determine when the search must stop, i.e. a TV station has been recognized.
The circuit operates with the following sequence (see fig. 10 for reference and explanation of pin 12 for speed definition):

1 - after pressing the search start key the search occurs in the Fast up mode

2 - subsequent transitions on pin 22 Stop/afc input are ignored during the first 15 search steps. After that the first M-H transition on the input preceded by at least one M-L transition will set the search into the Medium down (fast up/4) mode.
The acceptance delay of 15 search steps has been introduced to avoid the condition where the system could stop on the previous station (for example in the case the search start command has been given just before an AFC control command).

3 - the next M-L transition will switch the search to Slow up speed (67.7 Hz).
At this point the system is in normal AFC operation.

Fig. 10 – Automatic station capture diagram



B) **AFC operation:** when a station is perfectly tuned, the input signal coming from TDA 4431 is at middle level.
If the tuning moves lower than the threshold (below 38.9 MHz), the pin 22 goes low and the 13 bit internal counter is moved with Slow up speed to determine an increasing of the varicap voltage. When a detuning occurs in the opposite direction the input will go high and the tuning voltage is decreased with Slow down speed (8.4 Hz).
The increase or decrease of the tuning voltage is stopped as soon as the input returns to M level. Therefore during normal operation pin 22 acts as AFC control command.

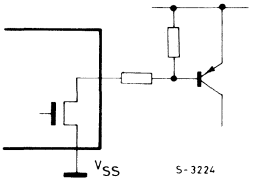
C) **Recall from memory:** when the circuit is in automatic operation mode and a pre-memorized program is recalled from Memory, a fixed value of 8 steps (≅ 31.2 mV) is subtracted from the tuning voltage. This corresponds to a detuning of about 0.6 MHz (UHF) and of 0.3 MHz in VHF III into that part of the IF response curve which corresponds to the fully transmitted sideband.
At this point the AFC operation takes over as described in point B) above and the exact tuning is reached in about 0.2 sec.
Due to this feature the AFC capture ratio will be increased and the requirements for stability of the tuner, of the reference voltage sources and of stability of the D/A converter are less severe.
In manual operation mode the memory content is instead read without any change.

Pins 23-24-25-26 - Band drive outputs

The information for band selection is present on these outputs, consisting of open drain transistors, one of which, in connection with the selected band, is conducting (see fig. 11).
The relations between pins and bands are as follows:

Pin 23 = VHF I
Pin 24 = VHF III
Pin 25 = UHF
Pin 26 = S

Fig. 11



Pin 27 - Mute output

A source follower transistor is provided to give a high level output during mute function.
The mute is present in the following cases:

- during automatic search. The mute is present 110 msec before the start of the search.
- during any program change for 320 msec.
  The mute is active 110 msec before the program change takes place.
- when the supply voltage V_{DD2} is applied, for about 320 msec.
- when the supply voltage V_{DD2} is removed.

Pin 28 - A) Automatic operation: search start
B) Manual operation: up/down search

This input is a three level one, i.e. it is normally in the middle level and the above mentioned functions are activated when it is connected to V_{DD2} or to GND.
The input is kept at a voltage corresponding to about the half of the supply voltage by an internal divider made with two resistors of about 1 Mohm.

A) Automatic operation

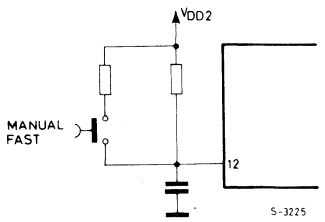
M193A - When the pin 28 is briefly connected to GND the search starts on the bands VHF III-UHF which are scanned in sequence. If it is connected to V_{DD2} the search is made on band VHF I and S. If the key is kept pushed, another search can start only by releasing the key and connecting is again to GND or V_{DD2}. If a Search start command is given while the system is already in search operation, the search is immediately stopped and after restarted on the new group of selected bands; the band where the system will search is that which has the same search speed of the previous one.
M193C, D-When the pin 28 is briefly connected to GND or to V_{DD2}, the search starts and remains in the previously selected band.
All types work as follows: if the key is kept pushed, another search can start only releasing the key and connecting it again to GND or V_{DD2}. During the search the tuning voltage is always changing from lower to higher voltage levels. The search is automatically stopped when the first station is found. The search is also stopped whenever a program change command is given. When the upper limit of the tuning voltage is reached, the search restarts from the lower limit of another band (M193A) or of the same band (M193C, D), after 210 msec of temporary stop. The search speed is determined by the RC network connected to pin 12.

B) Manual operation

When the input is connected to V_{DD2} the content of the internal counter is changed in such a way to have an increasing of the varicap voltage.
If the input is connected to GND the varicap voltage is decreased.
The search speed is determined by the RC network applied on pin 12.

Fast/low search speed is possible by changing the value of the same RC network (see fig. 12).
In manual operation the search is always made in the same band.
No inhibit of the search is provided when the lower or the upper limits of the varicap voltage are reached.
Step-by-step band selection is possible by temporarily connecting pin 2 to V_{DD2}.

Fig. 12



GENERAL INFORMATION

Command acceptance rules

1) When a manual command at pin 2, 3, 28 is given, an internal counter is immediately started. The command is accepted only after about 31 msec. of its continuous presence. If the command disappears before (for example in consequence of contact bouncing), the counter is immediately reset. When a command has been accepted, no other manual command is accepted until the previous command has been released.

2) Program change commands are immediately accepted and if the circuit is in the automatic search position, the search is stopped.
Manual commands given during the execution of the program change are not accepted except the automatic search start command.
This one is internally stored and executed at the end of the program change.

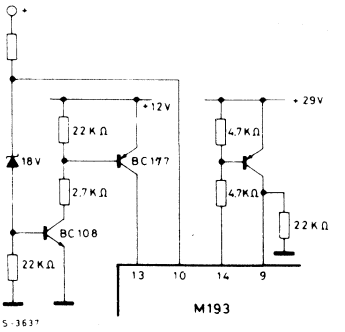
3) During the store cycle only the program change and the search start commands are accepted and executed at the end of the cycle.
The other commands are ignored.

Power-on sequence of supply voltages

To guarantee the correct reading of the memory at power-on the supply voltages must be applied as follows:

$$V_{DD1}\ (+18V),\ V_{DD2}\ (+12V)$$

The +18V must be higher than 16.5V 110 msec after the 12V is passed through the power-on reset threshold ($\simeq$ 6V).
From 0 to 6V the slew rate of the 12V is not important, from 6 to 10V the slew rate must not exceed 110 ms. If it is not possible to guarantee the availability of the 18V supply before the 12V we suggest using the following application.
It is recommended that the 29V is not applied when the 12V is not present. However there are no reliability problems if at power on and power off the 29V exists for a few seconds without the 12V supply being present.



MOS INTEGRATED CIRCUITS

M 258
M 259

PRELIMINARY DATA

RHYTHM GENERATORS

- 16 PROGRAMMABLE RHYTHMS (CODED FOR THE M258; ALSO AVAILABLE IN COMBINATION FOR THE M259
- 16 OUTPUTS (2 SECTIONS BY 8)
- MASK PROGRAMMABLE RESET COUNTS (24 or 32)
- DOWN BEAT OUT
- SYNC OUT
- EXTERNAL RESET
- TWO CHIP SELECTS (CS1, CS2) FOR SEPARATE TRISTATE CONDITION OF THE TWO OUTPUT SECTIONS
- INTERNAL PULL-UP ON THE INPUTS
- OPEN DRAIN OUTPUTS WITH RETURN TO "1" STATUS
- CHOICE BETWEEN RETURN TO "1" OR NOT ON 8 OUTPUTS (OUT 1, 2, 3, 4, 9, 10, 11, 12) SEPARATELY
- ONLY ONE POWER SUPPLY (+5V)
- VERY LOW POWER CONSUMPTION (150 mW TYP.)

The M258, M259 are monolithic rhythm generators specifically designed for electronic organs and other musical instruments.
Constructed on a single chip using MOS N-channel silicon gate technology, they are supplied in a 28 lead for (M258) or 40 lead for (M259) dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Source supply voltage	-0.3 to +7	V
V_i**	Input voltage	-0.3 to +7	V
I_o	Output current (at any pin)	3	mA
V_{OH}	Output voltage	12	V
T_{stg}	Storage temperature range	-65 to +125	°C
T_{op}	Operating temperature range	0 to 50	°C

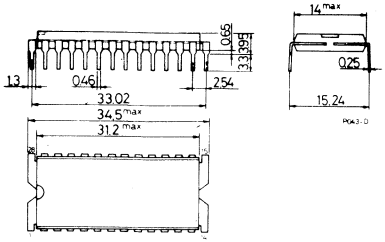
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

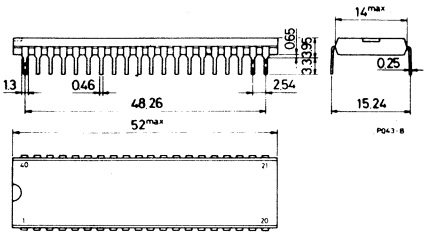
ORDERING NUMBERS: M258 B1/EB1 for dual in-line plastic package
M259 B1/EB1 for dual in-line plastic package

MECHANICAL DATA (dimensions in mm)

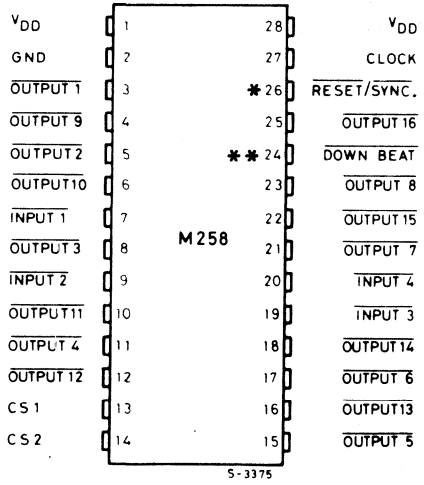
Dual in-line plastic package (28 lead)



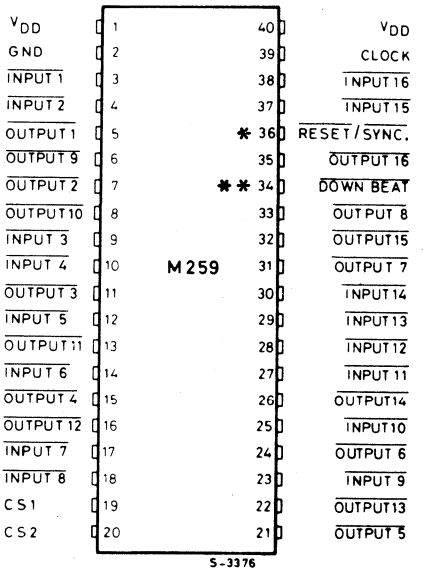
Dual in-line plastic package (40 lead)



PIN CONNECTIONS



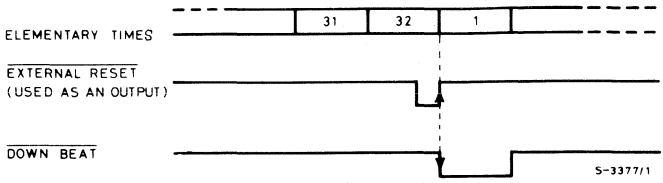
CS1 enables the outputs 01 to 08
CS2 enables the outputs 09 to 16



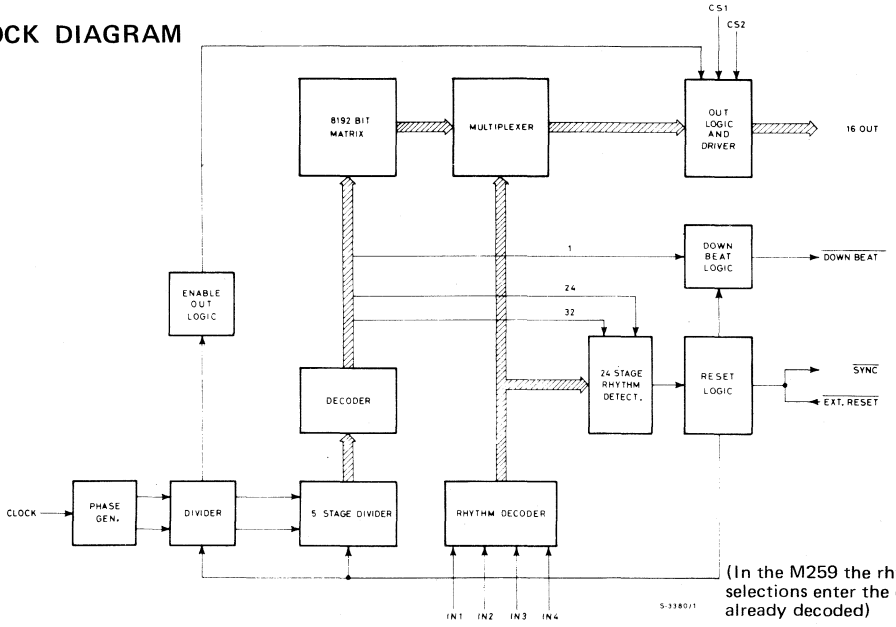
* This is a bidirectional pin. Used as an input it allows the chip reset; used as an output it can reset other devices.

** This pin generates a down beat trigger which can be used to drive an external lamp to indicate the first beat of the first bar of each rhythm.

RESET AND DOWN BEAT TIMING WAVEFORMS (POSITIVE LOGIC)



BLOCK DIAGRAM



(In the M259 the rhythm selections enter the chip already decoded)

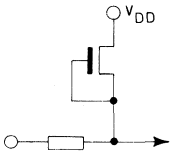
RHYTHM, SELECTION (for M258 only)

Rhythm	$\overline{IN4}$	$\overline{IN3}$	$\overline{IN2}$	$\overline{IN1}$
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

STATIC ELECTRICAL CHARACTERISTICS (positive logic, V_{DD}= 4.75 to 5.25V, T_{amb}= 0 to 50°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
CLOCK INPUT							
V_{IH}	Clock high voltage			2.4		V_{DD}	V
V_{IL}	Clock low voltage			0		0.4	V
DATA INPUTS							
V_{IH}	Input high voltage			2.4		V_{DD}	V
V_{IL}	Input low voltage			0		0.4	V
R_{IN}	Internal resistance to V_{DD}	V_I = 0V	V_{DD}= 5V	100	180		KΩ
I_{OL}(*)	Input load current	$V_I = V_{IL}$			-50		μA
EXT. RESET							
V_{IH}	Input high voltage			4.5		V_{DD}	V
V_{IL}	Input low voltage			0		1.5	V
R_{OFF}	Internal resistance to V_{DD} (inactive sync)	V_O= 0	V_{DD}= 5V	100	180		KΩ
R_{ON}	Internal resistance to V_{DD} (active sync)	V_O= 1V	V_{DD}= 4.75V		260	300	Ω
OUTPUTS (O_i, Down beat)							
R_{ON}		V_O= 1V			260	300	Ω
V_{OL}		Source current = 1 mA			0.26	0.3	V
I_{LO}		V_O= 12V	T_{amb}= 25°C			10	μA
POWER DISSIPATION							
I	Supply current	T_{amb}= 25°C			30		mA

(*) The "High Level" is clamped by the internal pull-up.

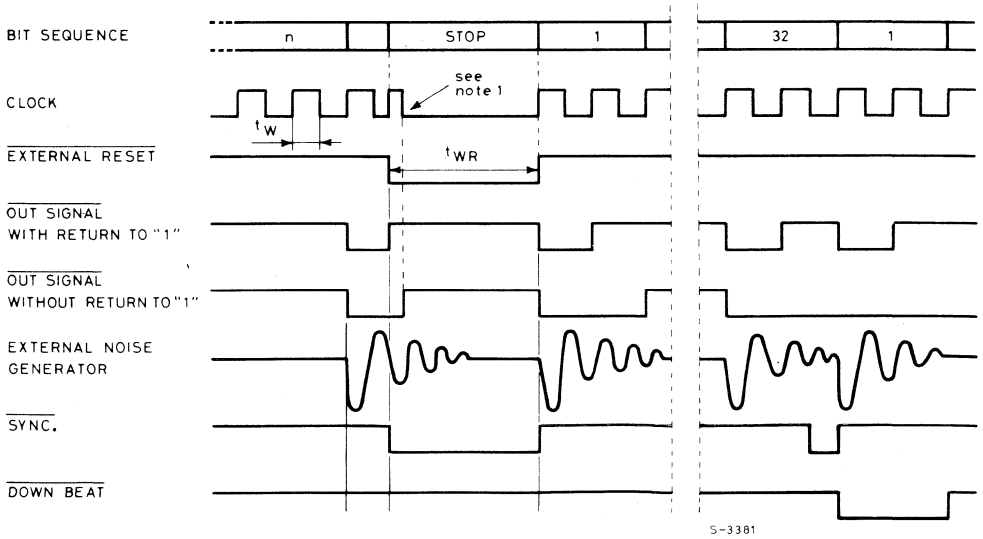


S-3382/1

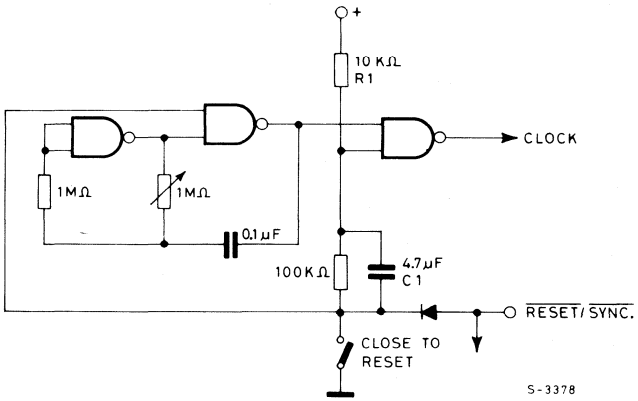
DYNAMIC ELECTRICAL CHARACTERISTICS (positive logic, V_{DD}= 4.75 to 5.25V, T_{amb}= 0 to 50°C unless otherwise specified)

Parameter		Test condistions	Values			Unit
			Min.	Typ.	Max.	
CLOCK INPUT						
f	Clock repetition rate		DC		100	KHz
t_w	Pulse width	Measured at 50% of the swing	5			µs
t_r	Rise time	Measured between 10% and 90% of the swing			100	µs
t_f	Fall time	Measured between 10% and 90% of the swing			100	µs
EXT. RESET						
t_{wR}	Pulse width		100			µs
t_{CR}	Clock delay with respect to reset		0			µs

TIMING WAVEFORMS

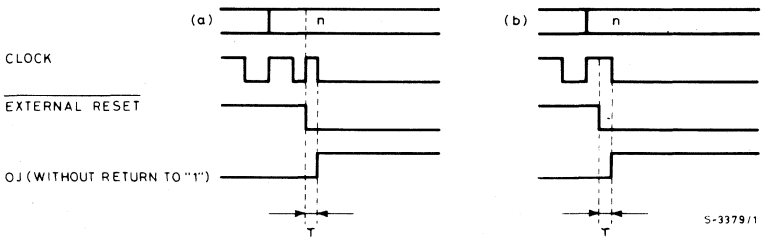


Note 1: This additional pulse, to reset the outputs without return to "1", can be obtained by using a clock generator as shown in the following diagram:



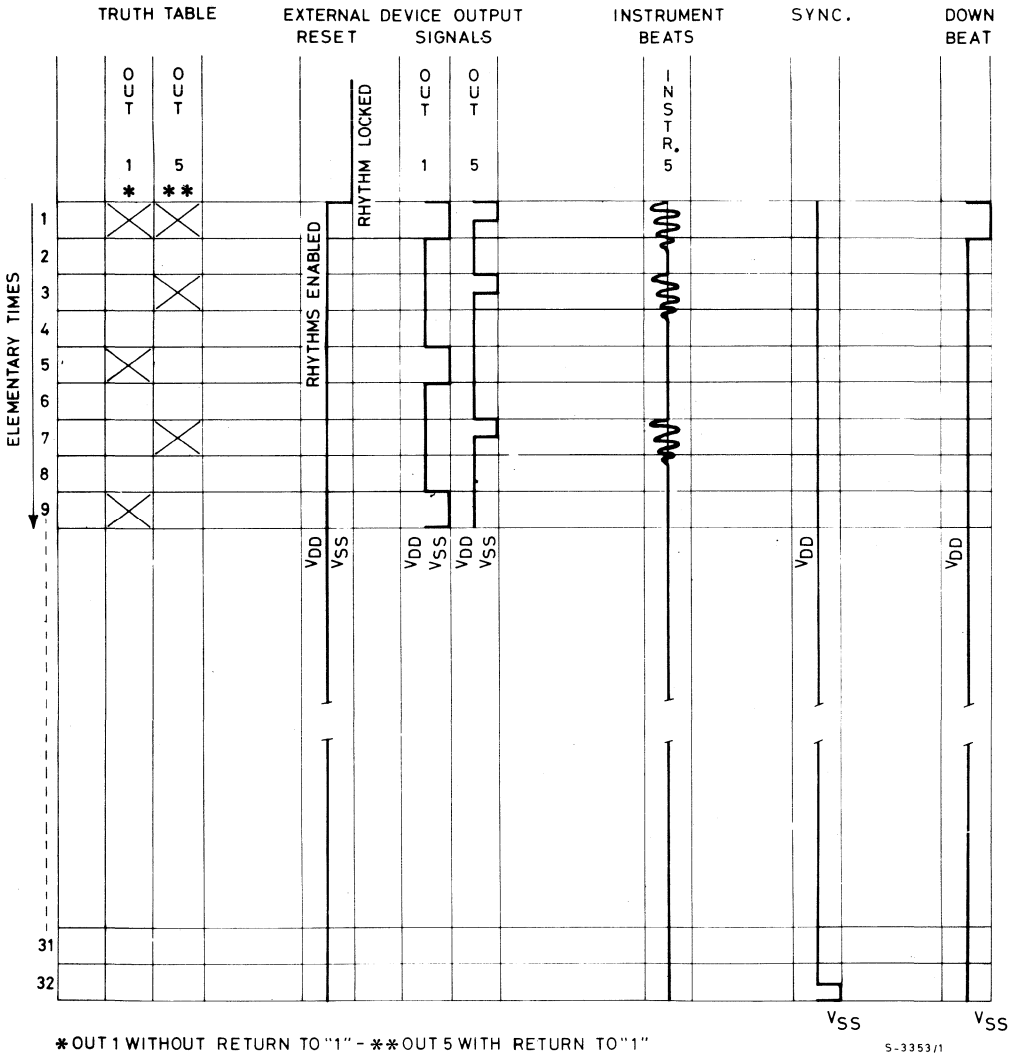
Ext. Reset/Sync. is a bidirectional pin. Used as an input it can reset the circuit as shown in the timing diagram and used as an output it can drive the reset of other devices.

Using the clock generator shown in the above figure, when the switch is closed asynchronous with respect to the clock, it is possible to have to two cases (see the following diagrams); in both the cases the output reset can be obtained by CS1 and CS2.

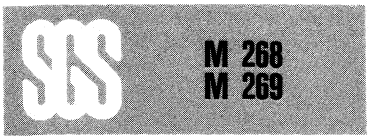


In both the cases the delay τ (in the outputs without return to "1") is defined through the constant R1 C1 $\geqslant$ 10 μsec.

INSTRUMENT BEATS VERSUS RHYTHM PROGRAM



Note: The outputs 01 to 08 are enabled by CS1; the outputs 09 to 16 are enabled by CS2. The outputs 01 to 04 and 09 to 12 are programmable separately without return to "1".



PRELIMINARY DATA

RHYTHM GENERATORS

- 16 CODED PROGRAMMABLE RHYTHMS FOR THE M268
- 8 PROGRAMMABLE RHYTHMS (ALSO AVAILABLE IN COMBINATION) FOR THE M269
- 12 OUTPUTS (2 SECTIONS 8 + 4)
- MASK PROGRAMMABLE RESET COUNTS (24 or 32)
- EPROM TECHNOLOGY PIN-TO-PIN COMPATIBLE DEVICE AVAILABLE FOR THE M268
- DOWN BEAT OUT
- SYNC OUT
- EXTERNAL RESET
- TWO CHIP SELECTS (CS1, CS2) FOR SEPARATE TRISTATE CONDITION OF THE TWO OUT. PUT SECTIONS
- INTERNAL PULL-UP ON THE INPUTS
- OPEN DRAIN OUTPUTS WITH RETURN TO "1" STATUS
- CHOICE BETWEEN RETURN TO "1" OR NOT ON 8 OUTPUTS (OUT 1, 2, 3, 4, 9, 10, 11, 12) SEPARATELY
- ONLY ONE POWER SUPPLY (+5V)
- VERY LOW POWER CONSUMPTION (150 mW TYP.)

The M268, M269 are monolithic rhythm generators specifically designed for electronic organs and other musical instruments.
Constructed on a single chip using MOS N-channel silicon gate technology, they are supplied in a 24 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Source supply voltage	-0.3 to +7	V
V_i **	Input voltage	-0.3 to +7	V
I_o	Output current (at any pin)	3	mA
V_{OH}	Output voltage	12	V
T_{stg}	Storage temperature range	-65 to +125	°C
T_{op}	Operating temperature range	0 to 50	°C

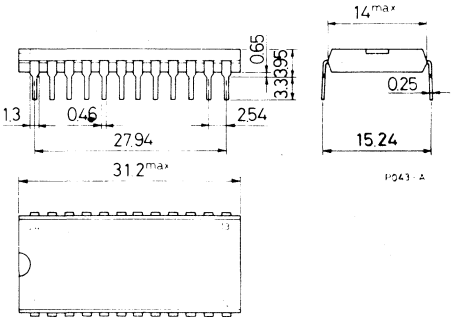
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

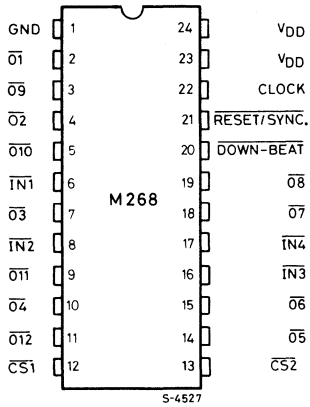
ORDERING NUMBERS: M268 B1/EB1 for dual in-line plastic package
M269 B1 for dual in-line plastic package

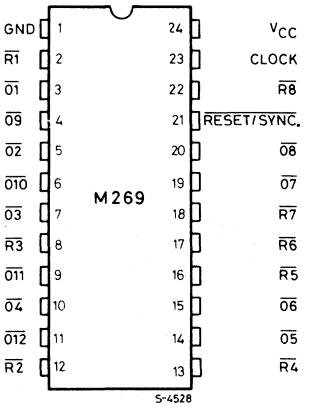
MECHANICAL DATA (dimensions in mm)

Dual in-line plastic package (24 lead)



PIN CONNECTIONS



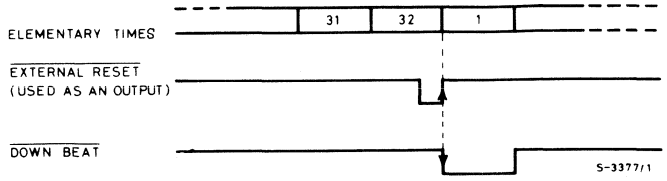


CS1 enables the outputs 01 to 08
CS2 enables the outputs 09 to 12

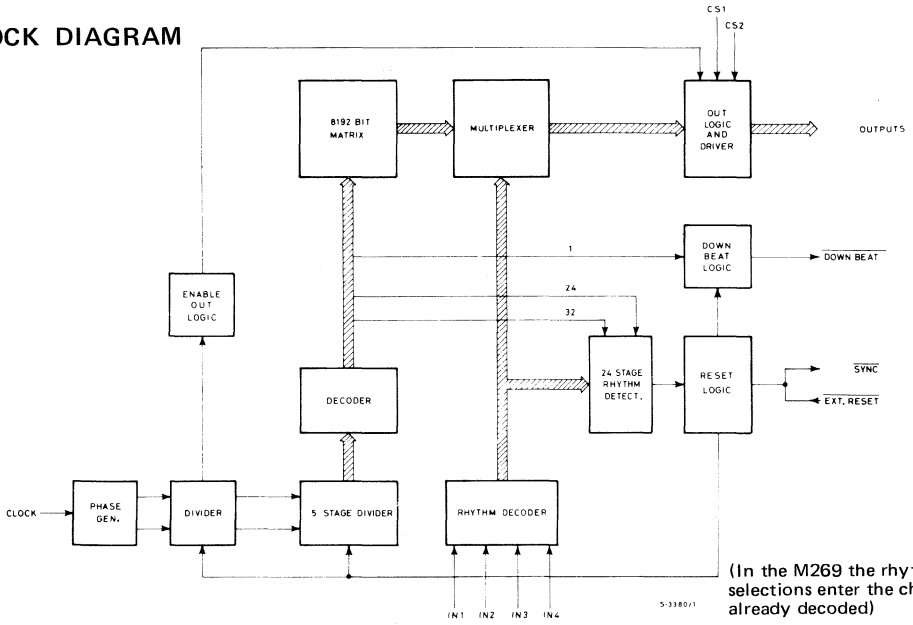
* This is a bidirectional pin. Used as an input it allows the chip reset; used as an output it can reset other devices.

** This pin generates a down beat trigger which can be used to drive an external lamp to indicate the first beat of the first bar of each rhythm.

RESET AND DOWN BEAT TIMING WAVEFORMS (POSITIVE LOGIC)



BLOCK DIAGRAM



(In the M269 the rhythm selections enter the chip already decoded)

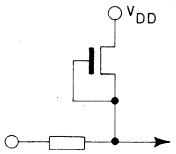
RHYTHM, SELECTION (for M268 only)

Rhythm	$\overline{IN4}$	$\overline{IN3}$	$\overline{IN2}$	$\overline{IN1}$
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1
10	0	1	1	0
11	0	1	0	1
12	0	1	0	0
13	0	0	1	1
14	0	0	1	0
15	0	0	0	1
16	0	0	0	0

STATIC ELECTRICAL CHARACTERISTICS (positive logic, V_{DD}= 4.75 to 5.25V, T_{amb}= 0 to 50°C unless otherwise specified)

Parameter		Test conditions		Values			Unit
				Min.	Typ.	Max.	
CLOCK INPUT							
V_{IH}	Clock high voltage			2.4		V_{DD}	V
V_{IL}	Clock low voltage			0		0.4	V
DATA INPUTS							
V_{IH}	Input high voltage			2.4		V_{DD}	V
V_{IL}	Input low voltage			0		0.4	V
R_{IN}	Internal resistance to V_{DD}	V_I = 0V	V_{DD}= 5V	100	180		KΩ
I_{OL}(*)	Input load current	$V_I = V_{IL}$			-50		μA
EXT. RESET							
V_{IH}	Input high voltage			4.5		V_{DD}	V
V_{IL}	Input low voltage			0		1.5	V
R_{OFF}	Internal resistance to V_{DD} (inactive sync)	V_O= 0	V_{DD}= 5V	100	180		KΩ
R_{ON}	Internal resistance to V_{DD} (active sync)	V_O= 1V	V_{DD}= 4.75V		260	300	Ω
OUTPUTS (O_i, Down beat)							
R_{ON}		V_O= 1V			260	300	Ω
V_{OL}		Source current = 1 mA			0.26	0.3	V
I_{LO}		V_O= 12V	T_{amb}= 25°C			10	μA
POWER DISSIPATION							
I	Supply current	T_{amb}= 25°C			30		mA

(*) The "High Level" is clamped by the internal pull-up.

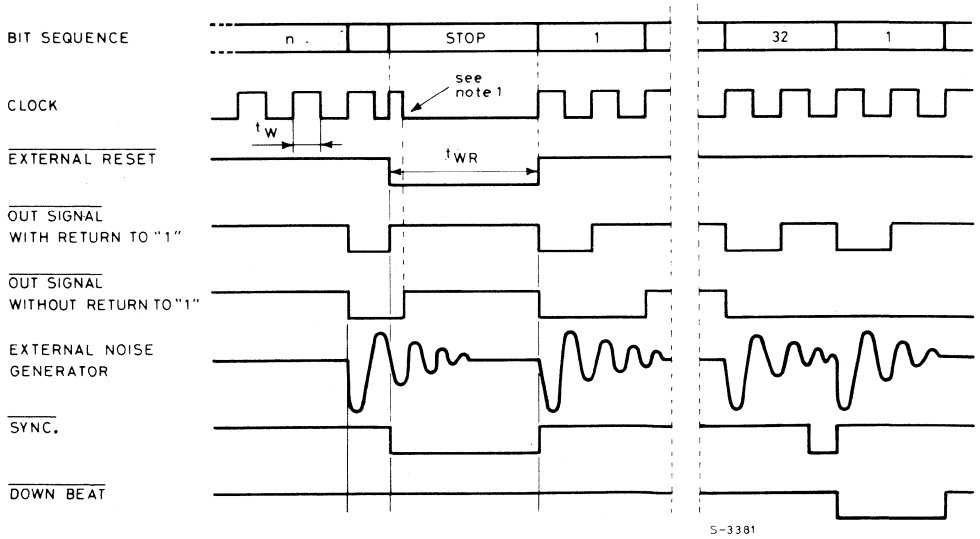


S-3382/1

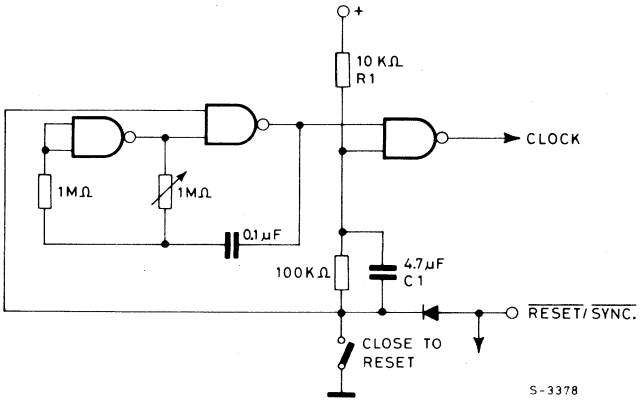
DYNAMIC ELECTRICAL CHARACTERISTICS (positive logic, V_{DD}= 4.75 to 5.25V, T_{amb}= 0 to 50°C unless otherwise specified)

Parameter		Test condistions	Values			Unit
			Min.	Typ.	Max.	
CLOCK INPUT						
f	Clock repetition rate		DC		100	KHz
t_w	Pulse width	Measured at 50% of the swing	5			µs
t_r	Rise time	Measured between 10% and 90% of the swing			100	µs
t_f	Fall time	Measured between 10% and 90% of the swing			100	µs
EXT. RESET						
t_{WR}	Pulse width		100			µs
t_{CR}	Clock delay with respect to reset		0			µs

TIMING WAVEFORMS

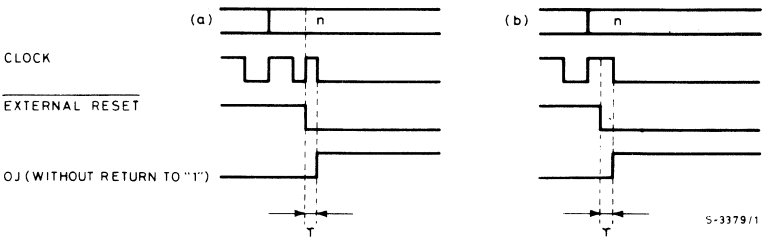


Note 1: This additional pulse, to reset the outputs without return to "1", can be obtained by using a clock generator as shown in the following diagram:



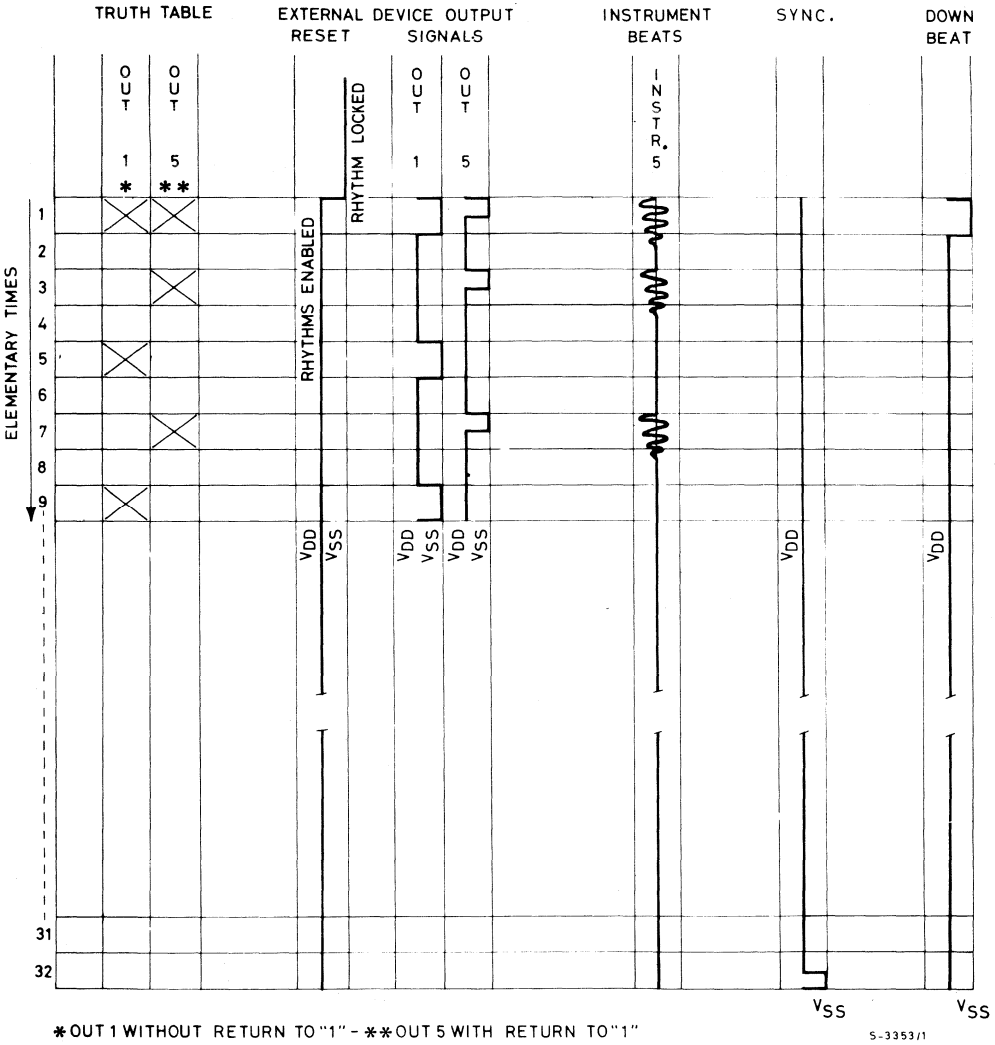
Ext. Reset/Sync. is a bidirectional pin. Used as an input it can reset the circuit as shown in the timing diagram and used as an output it can drive the reset of other devices.

Using the clock generator shown in the above figure, when the switch is closed asynchronous with respect to the clock, it is possible to have to two cases (see the following diagrams); in both the cases the output reset can be obtained by CS1 and CS2.



In both the cases the delay τ (in the outputs without return to "1") is defined through the constant R1 C1 $\geqslant$ 10 μsec.

INSTRUMENT BEATS VERSUS RHYTHM PROGRAM



Note: The output 01 to 08 are enabled by CS1; the outputs 09 to 12 are enabled by CS2. The outputs 01 to 04 and 09 to 12 are programmable separately without return to "1".

MOS INTEGRATED CIRCUITS

X CARD
M 274

PRELIMINARY DATA

PROGRAMMABLE ELECTRONIC CREDIT CARD

- LOW COST PLASTIC CREDIT CARD STYLE PACKAGING
- BUILT-IN CHIP WITH 105 CREDIT CELLS, ALL SEPARATELY ADDRESSABLE
- ONE SECURITY KEY WORD OF 8 BITS PROTECTED BY A SECURITY FUSE
- ONE MASK-PROGRAMMABLE 8-BIT CODE FOR USER IDENTIFICATION
- TYPICAL 10V POWER SUPPLY, 25V PROGRAMMING VOLTAGE
- LOW POWER CONSUMPTION: 115 mW (READING MODE), 320mW (PROGRAMMING MODE)
- WELL PROVEN NON-VOLATILE MEMORY DESIGN WITH 100 YEAR DATA RETENTION

This device is a remarkable new programmable memory product designed for electronic credit and identification cards. The product has only 7 connections (6 for user interfacing) and is essentially an EPROM of 17x8 bits.
If the XCARD is used as a credit card, the bit cells of the EPROM are all erased (content logic high) when the device is first delivered, and represent credit for services. Each time the card is used some bit cells are written, becoming useless. At any time the card can be checked for the amount of credit remaining and the reader can display this value.
When the XCARD is used as an identity card, it can be programmed with any one of several different codes (up to 2^{105}). This code can be read at any time by using an appropriate reader.
Row 16 of the matrix holds a mask programmable 8 bit code which can identify up to 256 different users. Since it is programmed during fabrication this code word is unerasable.
A second 8 bit word is used as a security key to detect fraudulent erasure and prevent re-use of the card.
This device is available in a plastic credit card style format (XCARD) or in a 14-lead plastic DIP for sampling and prototyping purposes (M274).

ABSOLUTE MAXIMUM RATINGS*

	Voltage on any pin (except PR)	-0.5 to 20	V
V_{PR}	Voltage on PR	-0.5 to 27	V
I_O	Output current	4	mA
P	Power dissipation	500	mW
T_{op}	Operating temperature range (XCARD only)	-30 to 60	°C
T_{stg}	Storage temperature range (XCARD only)	-30 to 60	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

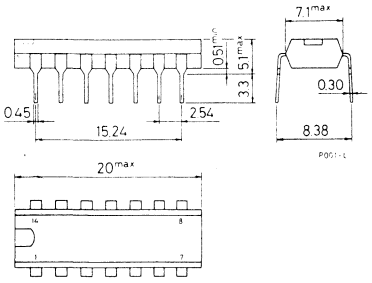
ORDERING NUMBERS

XCARD for credit card style package
M274B1 for dual in-line plastic package (samples only for evaluation)

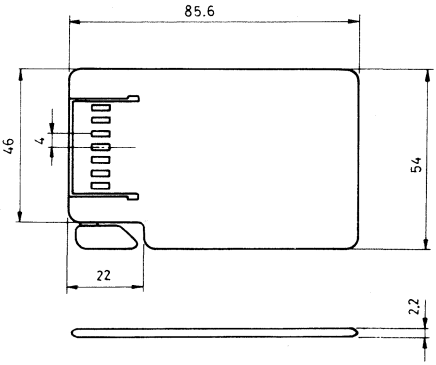
X CARD M 274

MECHANICAL DATA (dimensions in mm)

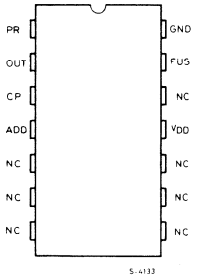
Dual in-line plastic package

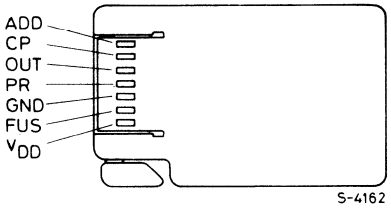


Plastic credit card style package



PIN CONNECTIONS



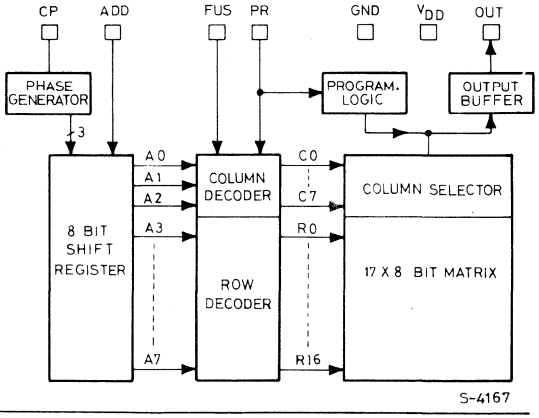


PIN DESCRIPTION

ADD	Address code input
CP	Clock input
PR	Programming signal input
OUT	Output
V_{DD}	Supply
GND	Ground
FUS*	Protection fuse
NC	Not connected

* Not connected
(see security key description)

BLOCK DIAGRAM



OPERATION

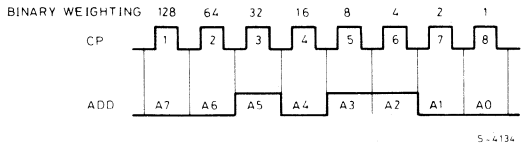
The matrix of 17 words by 8 bits must be addressed by serially loading an internal 8 bit shift register. The parallel outputs A0-A7 are decoded by the column and row decoders to address a single bit cell of the memory matrix. The content of this cell is output via an internal buffer. The logic of the M274 output is:

output = logic low (< 0.8V) = cell bit debited (written)
output = logic high (output transistor off) = cell bit in credit (unwritten)

The output is an open drain MOS transistor. During read operation the PR input is externally connected via a diode to the supply as shown in the application circuit, the current consumption is 10 mA (max) for V_{DD} = 10V.
The address data is loaded using an external clock of up to 100 kHz to read in the address bits A7 to A0 with clock pulses 1-8. When a frequency of less than 100 KHz is used, it is important to ensure that the mark time (i.e. CP pulse width) lies within the range 3 to 6 μs.
After the 8th clock pulse the output data is valid in 2 μs. Writing a bit cell is achieved by the application of a single +25V/10 mA pulse, of length 50 ms, to the PR input (> 10 μs after clock bit 8).

ADDRESSING

The serial address is obtained by generating a 1 or 0 in correspondence with one of 8 consecutive clock pulses. If for example cell number 44 is to be addressed (i.e. R5, C4 - see 17x8 BIT MATRIX ORGANIZATION), the correspondence between the two signals CP and ADD must be as shown below:



The 8-bit word corresponding to address 44 is therefore:

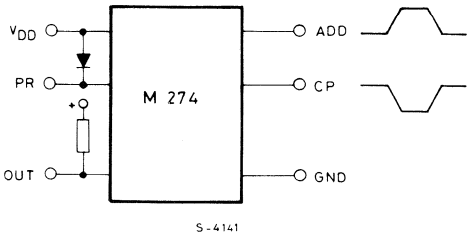
A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	1	1	0	0

Note: The first cell (i.e. R0, C0) is considered number 0.

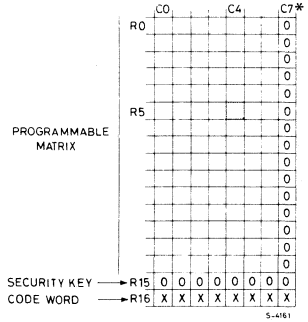
SECURITY KEY

One row of the matrix is written with an 8 bit word at manufacture, after writing this word - or security key - the write circuits to this row are destroyed by blowing an on-chip fuse and it is not possible to mend this fuse.
If any attempt is made to erase the card, to regain the credit value, the security key will also be erased: since the service point is normally designed to check for a valid security key before providing services, and before debiting the card, this is a complete method of protection against fraudulent re-use of the card.

APPLICATION CIRCUIT



17x8 BIT MATRIX ORGANIZATION

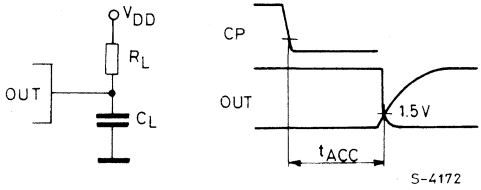


*C7 IS USED BY THE MANUFACTURER FOR TESTING

READING CHARACTERISTICS (see also timing waveforms)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		9		11	V
$V_{IL(ADD)}$	Address input low voltage		-0.3		0.5	V
$V_{IH(ADD)}$	Address input high voltage		8		V_{DD}	V
$V_{IL(CP)}$	Clock input low voltage		-0.3		0.5	V
$V_{IH(CP)}$	Clock input high voltage		8		V_{DD}	V
$V_{IL(PR)}$	Voltage on PR during verification		V_{DD}-0.8		V_{DD}-0.4	V
V_{OL}	Output low voltage	I_{OL}= 2 mA			0.8	V
I_{CP}	Clock input current (logic 0 and 1)				100	μA
I_{ADD}	Address input current (logic 0 and 1)				100	μA
I_{OL}	Output leakage current in OFF state	$V_O = V_{DD}$			100	μA
$I_{IL(PR)}$	Input current on PR during verification	$V_{PR} = V_{IL}$			5	mA
I_{DD}	Supply current				5	mA
f_{CP}	Clock frequency				100	kHz
$t_{s(ADD)}$	Address set-up time		0.5			μs
$t_{h(ADD)}$	Address hold time		0.5			μs
$t_{r(ADD)}$	Address rise time				2	μs
$t_{f(ADD)}$	Address fall time				2	μs
t_{ACC}	Access time	Note 1			2	μs
$t_{rCP)}$	Clock rise time				2	μs
$t_{f(CP)}$	Clock fall time				2	μs
$t_{w(CP)}$	CP pulse width		3		6	μs

Note 1 – t_{ACC} test conditions:
R_L= 5 kΩ, C_L= 100 pF, V_{DD}= 9V

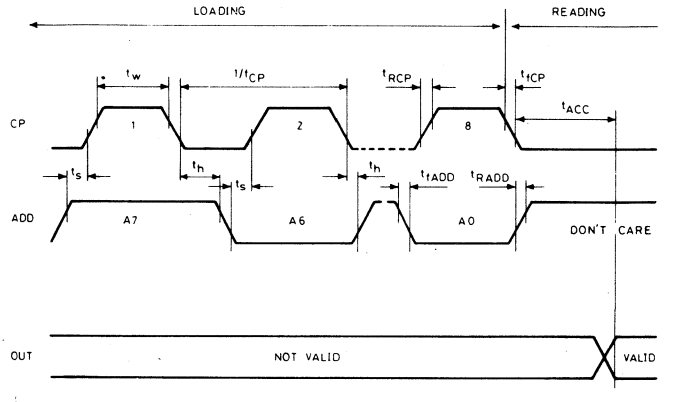


PROGRAMMING CHARACTERISTICS (see also timing waveforms)

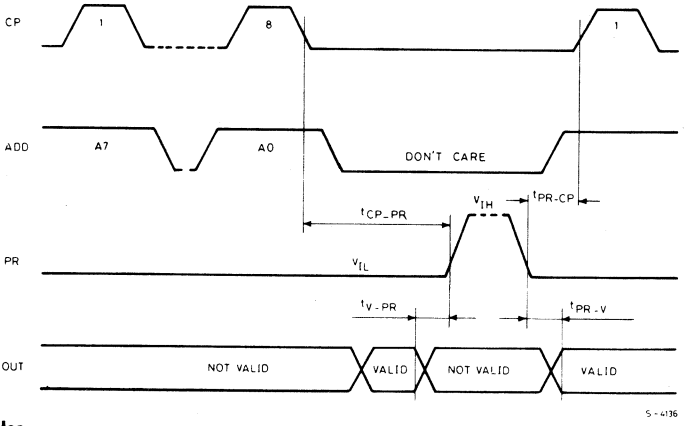
Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		9		11	V
$V_{IL(ADD)}$	Address input low voltage		-0.3		0.5	V
$V_{IH(ADD)}$	Address input high voltage		8		V_{DD}	V
$V_{IL(CP)}$	Clock input low voltage		-0.3		0.5	V
$V_{IH(CP)}$	Clock input high voltage		8		V_{DD}	V
$V_{IH(PR)}$	Voltage on PR during programming pulse		24		26	V
I_{CP}	Clock input current (logic 0 and 1)				100	μA
I_{ADD}	Address input current (logic 0 and 1)				100	μA
$I_{IH(PR)}$	Input current on PR	$V_{PR}= V_{IH}$			10	mA
I_{DD}	Supply current				5	mA
f_{CP}	Clock frequency				100	kHz
$t_{s(ADD)}$	Address set-up time		0.5			μs
$t_{h(ADD)}$	Address hold time		0.5			μs
$t_{r(ADD)}$	Address rise time				2	μs
$t_{f(ADD)}$	Address fall time				2	μs
$t_{r(CP)}$	Clock rise time				2	μs
$t_{f(CP)}$	Clock fall time				2	μs
$t_{w(CP)}$	CP pulse width		3		6	μs
$t_{r(PR)}$	Programming rise time		10		100	μs
$t_{f(PR)}$	Programming fall time		10		100	μs
$t_{w(PR)}$	PR pulse width		50			ms
t_{CP-PR}	Time between last CP pulse and PR		10			μs
t_{PR-CP}	Time between last PR pulse and CP		10			μs
t_{V-PR}	Time between valid output data and PR pulse		0			μs
t_{PR-V}	Time between end of PR pulse and valid output data		3			μs

TIMING WAVEFORMS

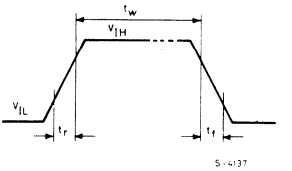
Reading



Programming



Programming pulse



MOS INTEGRATED CIRCUIT

M 702

16-STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{CC} (TYP.)
- INPUTS FULLY PROTECTED
- INVERTER AVAILABILITY IN CRYSTAL OSCILLATOR IMPLEMENTATION FOR TIMING APPLICATIONS

The **M 702 D2** (extended temperature range) and **M 702 D1/B1** (intermediate temperature range) are 16-stage binary counters constructed with COS/MOS technology in a single monolithic chip. The devices may be used as timing circuits the chips consists of 16-flip-flop, input inverter for use in a crystal oscillator, and an output buffer capable of driving standard stepping motors.
The device is available in 8-lead dual in-line miniature plastic package and 8-lead metal-can.

ABSOLUTE MAXIMUM RATINGS *

V_{DD}**	Supply voltage	-0.5 to	15	V
V_i	Input voltage (at any pin)	-0.5 to V_{DD}	+0.5	V
P_{tot}	Total power dissipation (per package)		200	mW
T_{stg}	Storage temperature	-65 to	150	°C
T_{op}	Operating temperature: for **D2** type	-55 to	125	°C
	for **D1/B1** type	-40 to	85	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** This voltage value are referred to V_{SS} pin voltage.

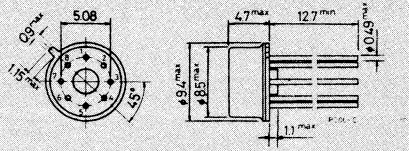
ORDERING NUMBERS:

M 702 **D2** for TO-99 metal can
M 702 **D1** for TO-99 metal can
M 702 **B1** for dual in-line plastic package

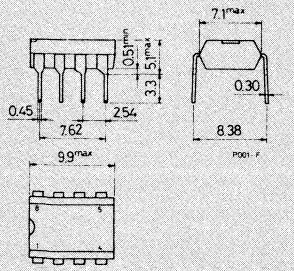
MECHANICAL DATA

Dimensions in mm

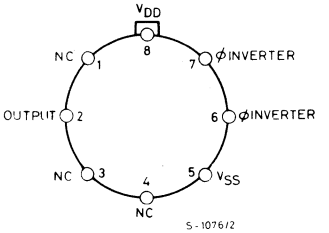
TO-99 metal can

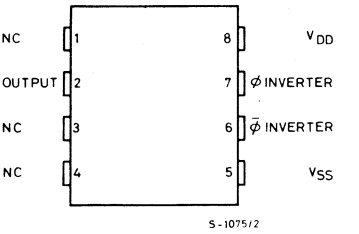


Dual in-line plastic package

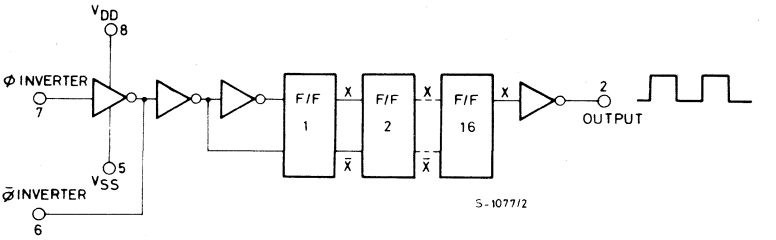


CONNECTION DIAGRAMS





LOGIC BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 15	V
	for crystal oscillator in clock applications	7 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **D2** type	-55 to 125	°C
	for **D1/B1** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

D2 type (extended temperature range)

Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-55°C			25°C			125°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_L	Quiescent supply current			5			15		0.5	15			900	μA
				10			25		1	25			1500	
				15			50		1	50			2000	
V_{OH}	Output high voltage	$I_O = 0$		5	4.99			4.99	5		4.95			V
				10	9.99			9.99	10		9.95			
V_{OL}	Output low voltage	$I_O = 0$		5			0.01		0	0.01			0.05	V
				10			0.01		0	0.01			0.05	
V_{NH}	Noise immunity			5	1.4			1.5	2.25		1.5			V
				10	2.9			3	4.5		3			
V_{NL}	Noise immunity			5	1.5			1.5	2.25		1.4			V
				10	3			3	4.5		2.9			
I_{DN}	Output drive current N-channel		0.5	5	12.5			12	15		8			mA
			0.5	10	18.5			18	20		14			
I_{DP}	Output drive current P-channel		4.5	5	-12.5			-12	-15		-8			mA
			9.5	10	-18.5			-18	-20		-14			
I_{IH},I_{IL}	Input leak.current	Any input		15			±1		$\pm 10^{-5}$	±1			±1	μA

D1/B1 types (intermediate temperature range)

Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_L	Quiescent supply current			5			50		1	50			700	μA
				10			100		2	100			1400	
				15			900		10	900			5000	
V_{OH}	Output high voltage	I_{OH}=0		5	4.99			4.99	5		4.95			V
				10	9.99			9.99	10		9.95			
V_{OL}	Output low voltage	I_{OL}=0		5			0.01		0	0.01			0.05	V
				10			0.01		0	0.01			0.05	
V_{NH}	Noise immunity			5	1.4			1.5			1.5			V
				10	2.9			3	4.5		3			
V_{NL}	Noise immunity			5	1.5			1.5	2.25		1.4			V
				10	3			3	4.5		2.9			
I_{DN}	Output drive current N-channel		0.5	5	12.5			12	15		8			mA
			0.5	10	18.5			18	20		14			
I_{DP}	Output drive current P-channel		4.5	5	-12.5			-12	-15		-8			mA
			9.5	10	-18.5			-18	-20		-14			
I_{IH},I_{IL}	Input leak.current	Any input		15			±1		$\pm 10^{-5}$	±1			±1	μA

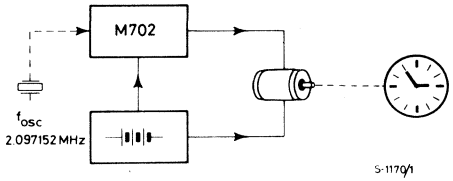
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 pF, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

Parameter		Test conditions	Values						Unit
			V_{DD} (V)	M 702 D2			M 702 D1/B1			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{WH}, t_{WL}	Minimum input pulse width		5		100	115		100	140	ns
			10		50	60		50	75	
t_r, t_f	Input clock rise and fall time		5			15			15	µs
			10			10			10	
f_{max}	Maximum clock frequency		5	4.4	5		8.5	10		MHz
			10	3.5	5		6.5	10		
C_I	Input capacitance	Any input			5			5		pF

TYPICAL APPLICATIONS

Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.
Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs.
Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.

Electronic watch application circuit



COS/MOS INTEGRATED CIRCUIT

M 706

PRELIMINARY DATA

16-STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 16V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY IN CRISTAL OSCILLATOR IMPLEMENTATION FOR TIMING APPLICATION

The **M 706** is a 16-stage binary counter constructed with COS/MOS technology on a single monolithic chip. The device may be used as timing circuit. It consists of 16 flip-flops, input inverter for use in a crystal oscillator and two output buffers providing push-pull bridge operation. The device is available in 8-lead minidip.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to 16	V
V_I	Input voltage (at any pin)	-0.5 to V_{DD} +0.5	V
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	-40 to 85	°C

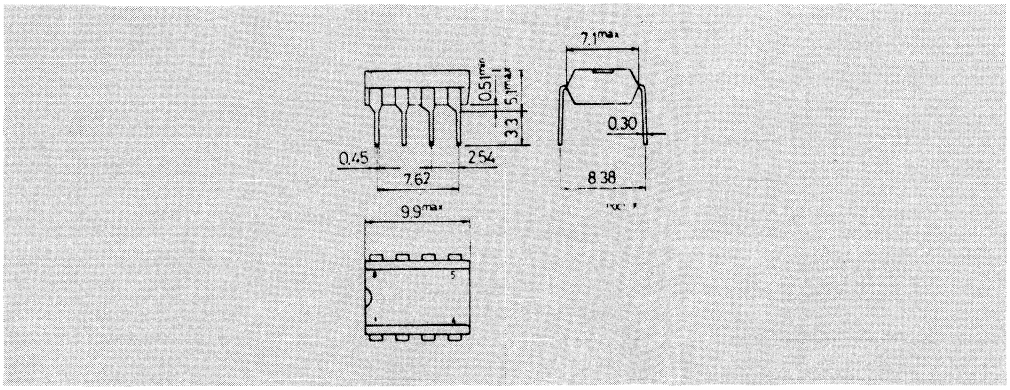
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** This voltage is with respect to V_{SS} (GND) pin voltage.

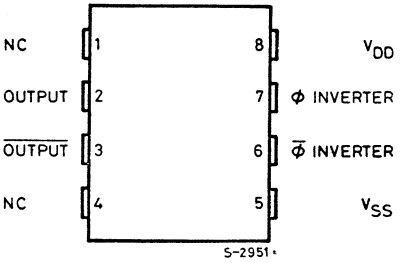
ORDERING NUMBER: M 706 B1

MECHANICAL DATA

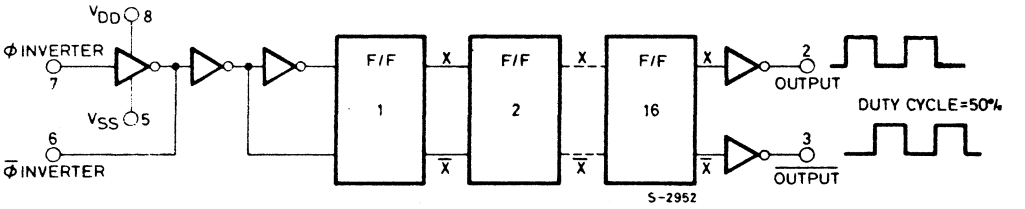
Dimensions in mm



PIN CONNECTIONS



LOGIC BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

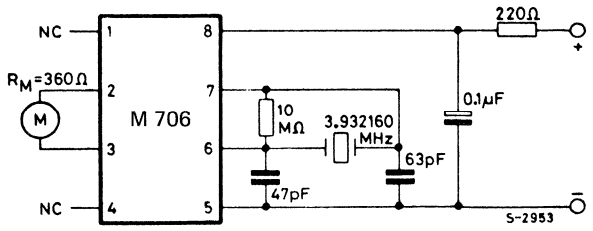
V_{DD}	Supply voltage: for general applications	3 to 15	V
	for crystal oscillator in clock application	7 to 15	V
V_i	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions			Values at 25°C			Unit
			V_o (V)	V_{DD}(V)	Min.	Typ.	Max.	
I_L	Quiescent supply current			5		1	50	μA
				10		2	100	
V_{OH}	High output voltage	I_O= 0		5	4.99	5		V
				10	9.99	10		
V_{OL}	Low output voltage	I_O= 0		5		0	0.01	V
				10		0	0.01	
I_{DN}	Output drive current N-channel		0.5	5	6	7.5		mA
			0.5	10	9	10		
I_{DP}	Output drive current P-channel		4.5	5	-6	-7.5		mA
			4.5	10	-9	-10		

TYPICAL APPLICATION

Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.
Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile blocks, and digital timing references in any circuit requiring accurately timed outputs.
Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.



COS/MOS INTEGRATED CIRCUIT

M 714

PRELIMINARY DATA

23-STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 15V
- HIGH NOISE IMMUNITY: 45% of V_{DD} (TYP.)
- INPUTS FULLY PROTECTED
- OUTPUT WAVEFORMS SHAPED for a 25% DUTY CYCLE

The M714 (standard temperature range) is 23-stage binary counter constructed with MOS-P channel and N-channel enhancement mode devices in a single monolithic chip. The device may be used as timing circuit. It consist of 23 flip-flops, two output buffers, providing push-pull operation one zener diode providing transient protection at ~ 10V, and input inverters for use in a crystal oscillator. The device is available in 14-lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.5 to 15 V
V_i	Input voltage (at any pin)	$V_{SS} \leqslant V_i \leqslant V_{DD}$
P_{tot}	Total power dissipation (per package, including zener diode)	200 mW
T_{stg}	Storage temperature	-65 to 150 °C
T_{op}	Operating temperature	-40 to 85 °C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

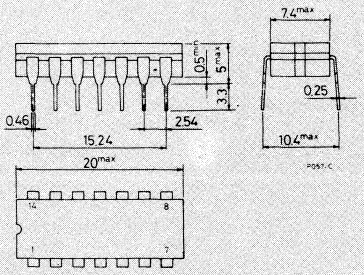
** With respect to V_{SS} (GND) pin.

ORDERING NUMBERS: M714 D1 for dual in-line ceramic package frit seal
M714 B1 for dual in-line plastic package

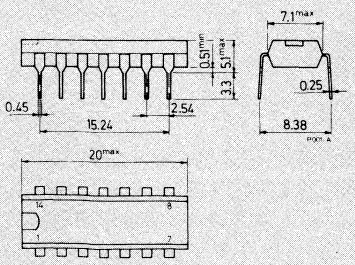
MECHANICAL DATA

Dimensions in mm

Dual in-line ceramic package, frit seal

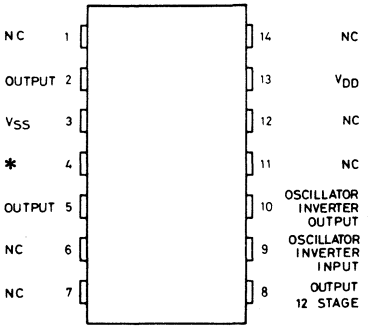


Dual in-line plastic package



M 714

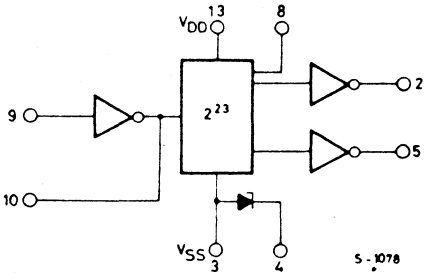
PIN CONNECTIONS



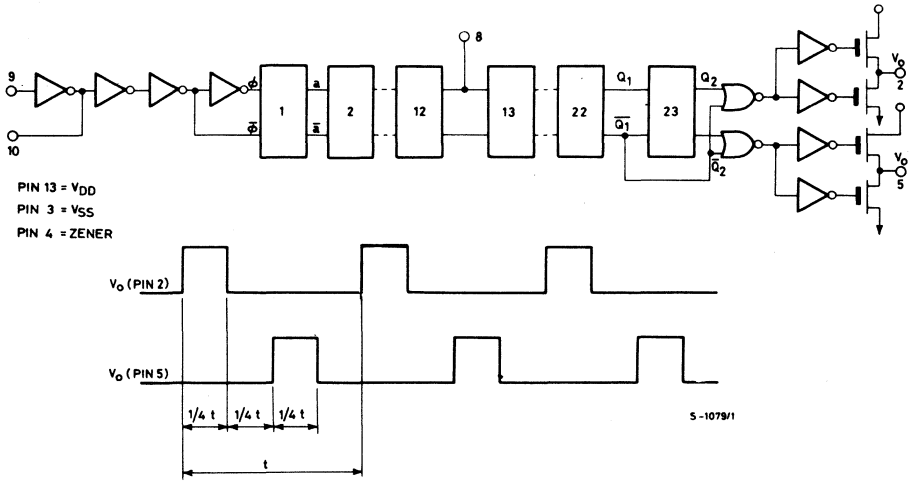
* ZENER CATHODE

S-1080/1

LOGIC DIAGRAM



BLOCK DIAGRAM and OUTPUT WAVEFORMS



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 15	V
	for oscillator starting	6 to 15	V
V_I	Input voltage	V_{DD} to V_{SS}	
T_{op}	Operating temperature	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

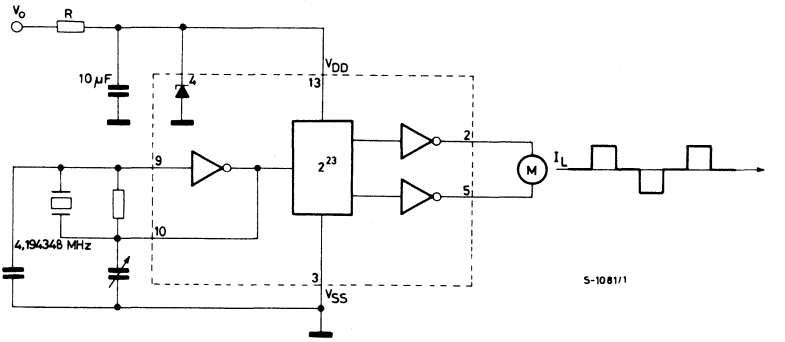
Parameter		Test conditions	V_O (V)	V_{DD} (V)	Values									Unit
					-40°C			25°C			85°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_L	Quiescent supply current			5			50		1	50			700	μA
				10			100		2	100			1400	
				15										
V_{OH}	Output high voltage	I_O= 0		5	4.99			4.99	5		4.95			V
				10	9.99			9.99	10		9.95			
V_{OL}	Output low voltage	I_O= 0		5			0.01		0	0.01			0.05	V
				10			0.01		0	0.01			0.05	
V_{NH}	Noise immunity			5	1.4			1.5	2.25		1.5			V
				10	2.9			3	4.5		3			
V_{NL}	Noise immunity		1	5	1.5			1.5	2.25		1.4			V
			1	10	3			3	4.5		2.9			
I_{DN}	Output drive current N-channel		0.5	5	2.2			1.8	4		1.3			mA
			0.5	10	3.5			2.8	8		2			
I_{DP}	Output drive current P-channel		4.5	5	-1.6			-1.3	-4		-0.9			mA
			9.5	10	-2.8			-2.3	-8		-1.6			
V_Z	Zener voltage	I_Z=100μA							10.5					V
		I_Z=10 mA							11.2					
I_{IH},I_{IL}	Input leakage curr.								10					pA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 15 pF, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns.

Parameter		Test conditions		Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_r, t_f	Input clock rise and fall time		5			15	μs
			10			10	
f_{CL}	Maximum clock input frequency		5	3.5	5		MHz
			10	6.5	10		
C_I	Input capacitance	Any input			5		pF

TYPICAL APPLICATIONS

Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.
Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs.
Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.



COS/MOS INTEGRATED CIRCUIT

M 730

PRELIMINARY DATA

23-STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 17V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY FOR CRYSTAL OSCILLATOR TIMING APPLICATION
- ADJUSTABLE FREQUENCY DIVIDER IN 127 STEPS
- TEST OUTPUT AVAILABLE
- MOTOR DRIVE STAGE OUTPUT

The M730 (standard temperature range) is a 23 stage binary counter in COS/MOS technology in a single monolithic chip. An inverter is available for crystal oscillator application in which the function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose, seven adjustment terminals are provided on the M730: they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 14. If one or more adjustment terminals are grounded (taken to pin 13), the output frequency decreases. The by-four-divided oscillator frequency may be checked at a separate test output (pin 8) non-reactive with respect to the oscillator. Based on this check the output frequency and consequently the accuracy of the clock may be adjusted at the terminal 1 to 7 by means of the variable frequency divider. With an oscillator frequency of 4.194812 MHz, the series-connected push-pull output stage supplies a symmetrical square wave signal with a pulse duty factor of 0.5 and a repetition frequency of 0.5 Hz if the variable frequency divider is set to its medium value. The device is available in 14 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.3 to +17	V
I_{11}	Output current	60	mA
P_{tot}	Power dissipation at $T_{amb} = 25°C$	200	mW
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +125	°C

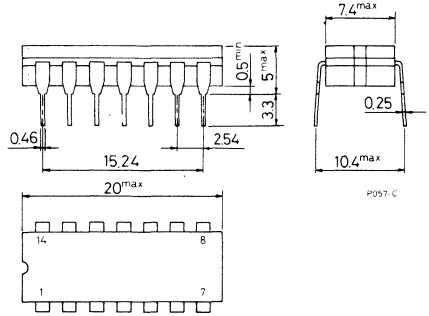
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

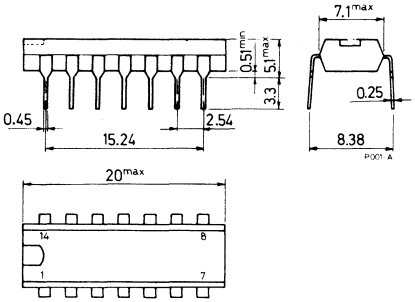
ORDERING NUMBERS: M730 B1 for dual in-line plastic package
M730 D1 for dual in-line ceramic package frit seal

MECHANICAL DATA (dimensions in mm)

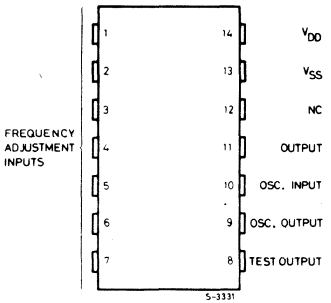
Dual in-line ceramic package frit seal



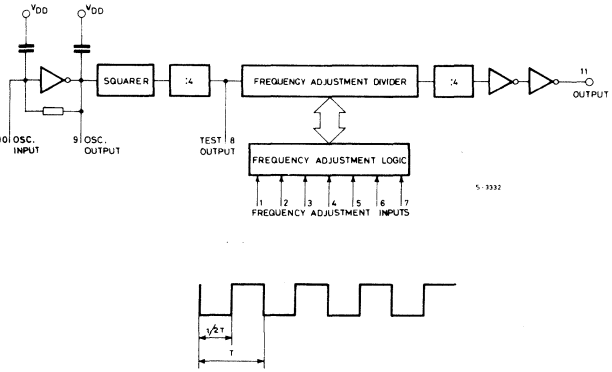
Dual in-line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM and OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 16.5	V
	for oscillator starting	6 to 16.5	V
V_i	Input voltage	V_{DD} to V_{SS}	V
I_{11}	Output current	40	mA
T_{op}	Operating temperature	-40 to +85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions			Values									Unit
					-40°C			25°C			85°C			
			V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output high voltage	I_{OH}= 0		6	5.99			5.99	6		5.95			V
				12	11.99			11.99	12		11.95			
V_{OL}	Output low voltage	I_{OL}= 0		6			0.01		0	0.01			0.05	V
				12			0.01		0	0.01			0.05	
I_{DN}	Output drive current N-channel		2	6	21			20	25		13			mA
			2	12	34			33	40		22			
I_{DP}	Output drive current P-channel		4	6	21			20	25		13			mA
			10	12	34			33	40		22			
I_{ON}	Current consump.	I_O= 0*		12					3					mA

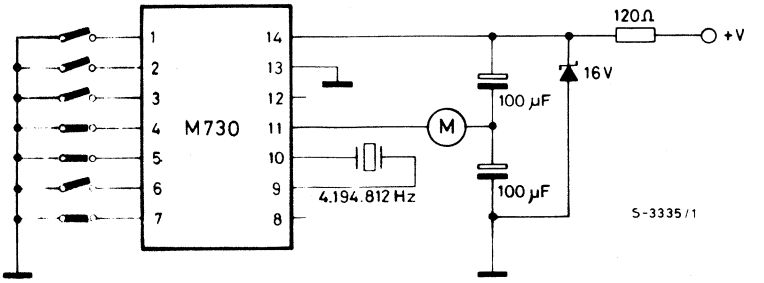
* At quartz frequency of 4.194.812 Hz.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, quartz frequency 4.194.812 Hz)

Parameter		Test conditions	V_{DD} (V)	Values						Unit
				M730 D1 type			M730 B1 type			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
f_T	Frequency test output		12		1.048703			1.048703		Hz
f_o**	Output frequency		12		0.5			0.5		Hz
$\frac{\Delta f_o}{f_o}$	Range output frequency adjustment		12		± 121			± 121		ppm
R_o	Output resistance	R_L= 300Ω	12			100			100	Ω

** At the centre position of the variable divider.

APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUIT

M 731

PRELIMINARY DATA

16-STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 17V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY FOR CRYSTAL OSCILLATOR TIMING APPLICATION
- ADJUSTABLE FREQUENCY DIVIDER IN 127 STEPS
- TEST OUTPUT AVAILABLE
- MOTOR DRIVE STAGE OUTPUT

The M731 (standard temperature range) is a 16 stage binary counter in COS/MOS technology in a single monolithic chip. An inverter is available for crystal oscillator application in which the function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose seven adjustment terminals are provided on the M731: they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 14. If one or more adjustment terminals are grounded (taken to pin 13), the output frequency decreases. The by-four-divided oscillator frequency may be checked at a separate test output (pin 8) non-reactive with respect to the oscillator. With an oscillator frequency of 4.194812 MHz, the series-connected push-pull output stage supplies a symmetrical square wave signal with a pulse duty factor of 0.5 and a repetition frequency of 64 Hz if the variable frequency divider is set to its medium value. The device is available in 14 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.3 to +17	V
I_{11}	Output current	60	mA
P_{tot}	Power dissipation at T_{amb}= 25°C	200	mW
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +125	°C

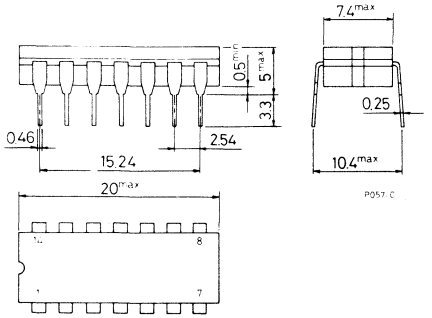
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

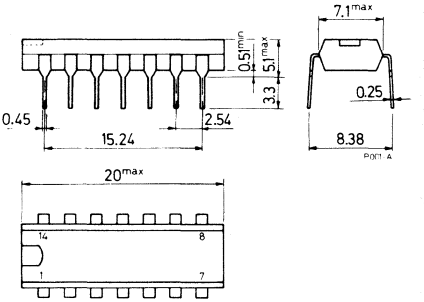
ORDERING NUMBERS: M731 B1 for dual in-line plastic package
M731 D1 for dual in-line ceramic package frit seal

MECHANICAL DATA (dimensions in mm)

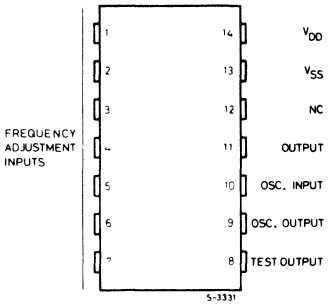
for dual in-line ceramic package, frit seal



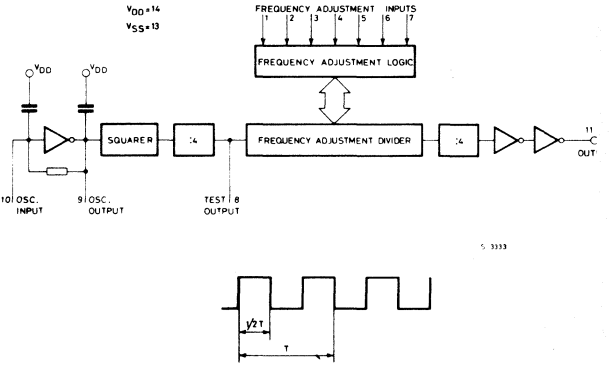
for dual in-line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM and OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 16.5	V
	for oscillator starting	6 to 16.5	V
V_i	Input voltage	V_{DD} to V_{SS}	V
I_{11}	Output current	40	mA
T_{op}	Operating temperature	-40 to +85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output high voltage	$I_{OH}= 0$		6	5.99			5.99	6		5.95			V
				12	11.99			11.99	12		11.95			
V_{OL}	Output low voltage	$I_{OL}= 0$		6			0.01		0	0.01			0.05	V
				12			0.01		0	0.01			0.05	
I_{DN}	Output drive current N-channel		2	6	21			20	25		13			mA
			2	12	34			33	40		22			
I_{DP}	Output drive current P-channel		4	6	-21			-20	-25		-13			mA
			10	12	-34			-33	-40		-22			
I_{ON}	Current consump.	$I_O= 0$*		12					3					mA

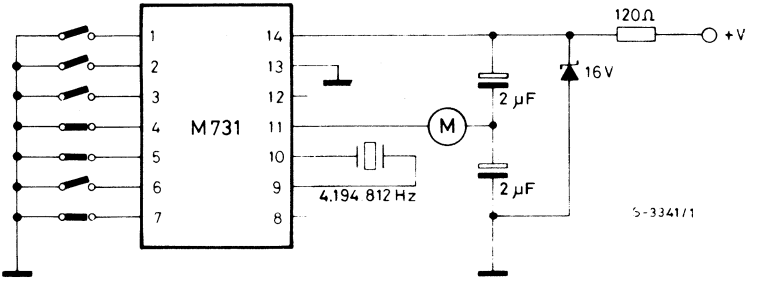
* At quartz frequency of 4.194.812 Hz.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, quartz frequency 4.194.812 Hz)

Parameter		Test conditions	V_{DD} (V)	Values						Unit
				M731 D1			M731 B1			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
f_T	Frequency test output		12		1.048703			1.048703		Hz
f_o**	Output frequency		12		64			64		Hz
$\frac{\Delta f_o}{f_o}$	Range output frequency adjustment		12		± 121			± 121		ppm
R_o	Output resistance	$R_L= 300\Omega$	12			100			100	Ω

** At the centre position of the variable divider.

APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUITS

M 738/M 740
M 741/M 747

PRELIMINARY DATA

7-STAGE DIVIDER

- LOW POWER DISSIPATION
- LOW OUTPUT IMPEDANCE ON BOTH HIGH AND LOW STATE
- WIDE SUPPLY VOLTAGE RANGE: 5 to 15V
- HIGH NOISE IMMUNITY
- INPUTS FULLY PROTECTED

The M738/M740/M741/M747 are integrated circuits constructed in COS/MOS technology for use as frequency dividers in electronic organs. All the devices consist of 7 stages of binary division connected to give five divider blocks for the M741/M747 and four divider blocks for the M738/M740. The information transfer occurs on the positive going edge of the clock, for M740 and M747, and the negative going edge of the clock for M738/M741, and each output features a symmetrical impedance buffer (300Ω typ. at V_{DD}= 10V). They are available in 14 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to	15	V
V_I	Input voltage (at any pin)	-0.5 to V_{DD}+0.5		V
P_{tot}	Total power dissipation (per package)		200	mW
T_{stg}	Storage temperature	-65 to	150	°C
T_{op}	Operating temperature	-40 to	85	°C

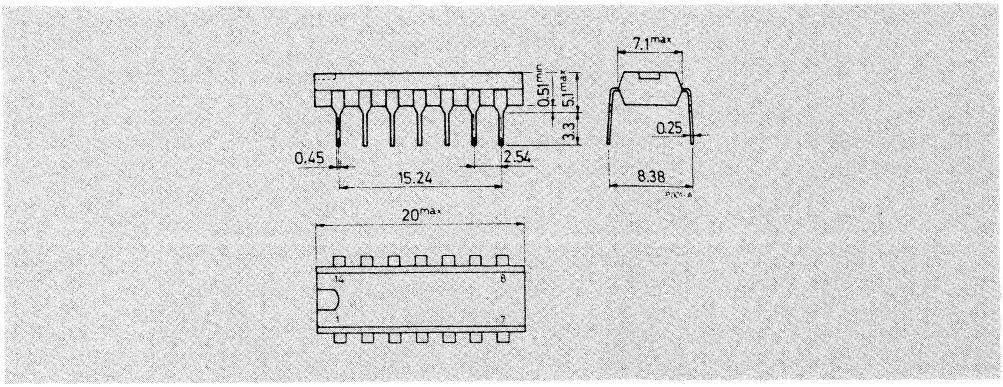
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages values are refered to V_{SS} pin voltage.

ORDERING NUMBERS: M 7XX B1 for dual in-line plastic package

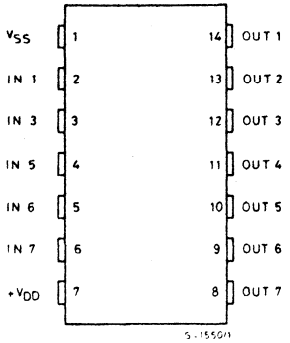
MECHANICAL DATA

Dimensions in mm



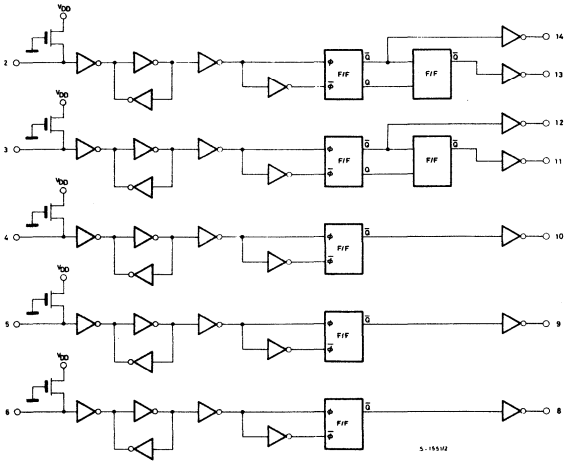
CONNECTION DIAGRAMS

For M741/M747

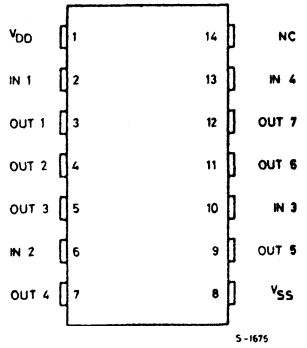


FUNCTIONAL DIAGRAMS

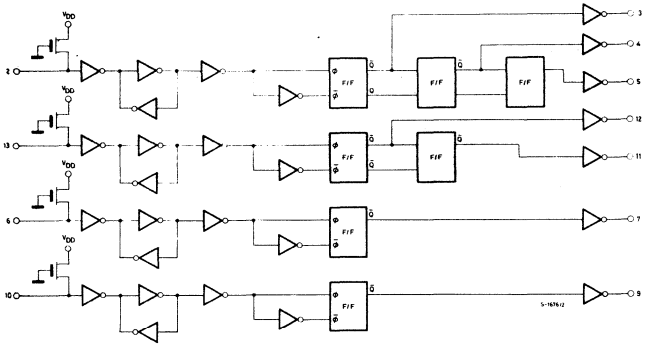
For M741/M747



For M738/M740



For M738/M740



RECOMMENDED OPERATING CONDITIONS

Parameter		V_{DD}(V)	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		5		15	V
V_I	Input voltage		-0.5		V_{DD}+0.5	V
T_{op}	Operating temperature		-40		85	°C
t_w	Width of clock pulse (high or low)	5		200		ns
		10		100		

STATIC ELECTRICAL CHARACTERISTICS (over recomended operating conditions)

Typical values are at T_{amb} = 25°C

Parameter	Test conditions			Values									Unit
		V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CCL} Quiescent supply current	V_i=V_{DD}		5			5			5			300	μA
			10			10			10			600	
			15			50			50			2000	
V_{OH} High level output voltage	I_o= 0		5	4.99			4.99			4.95			V
			10	9.99			9.99			9.95			
			15	14.99			14.99			14.95			
V_{OL} Low level output voltage	I_o= 0		5			0.01			0.01			0.05	V
			10			0.01			0.01			0.05	
			15			0.01			0.01			0.05	
I_{OL} Output drive current N-channel		0.5	5	0.5			0.5	0.8		0.45			mA
		0.5	10	1			1	1.6		0.95			
		0.5	15	1.6			1.6	2.5		1.55			
I_{OH} Output drive current P-channel		4.5	5	-0.5			-0.5	-0.8		-0.45			mA
		9.5	10	-1			-1	-1.6		-0.95			
		14.5	15	-1.6			-1.6	-2.5		-1.55			
I_{IL} Input current	V_i= 0		15				3	30	100				μA
I_{IH} Input current	V_i=V_{DD}		15			1			1			1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Parameter		Test conditions		Values			Unit
			V_{DD}(V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time from inputs to:	1 division stage outputs	C_L = 15 pF on all outputs see timing diagram	5			500	ns
			10			250	
	2 division stage outputs		5			1000	ns
			10			500	
	3 division stage outputs		5			1500	ns
			10			750	
t_{TLH}, t_{THL} Output transition time			5			500	ns
			10			250	
f_{max} Maximum toggle frequency		C_L= 15 pF on all outputs	5	0.6	2.5		MHz
			10	2	5		
* Cross talk immunity level					70		dB
C_I Input capacitance					5		pF

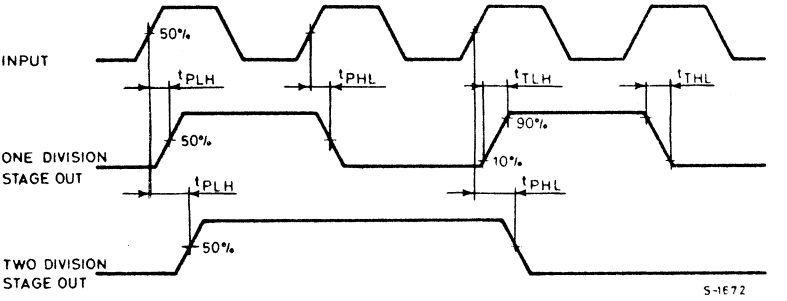
* Send a frequency of 20 kHz to input V_{I1} charge output V_{O1} with 5 kΩ and 15 pF, measure the level of the 10 kHz frequency present at all outputs.

Cross talk level = $20 \log \frac{V_{O1}\ (10\ kHz)}{V_{OX}\ (10\ kHz)}$.

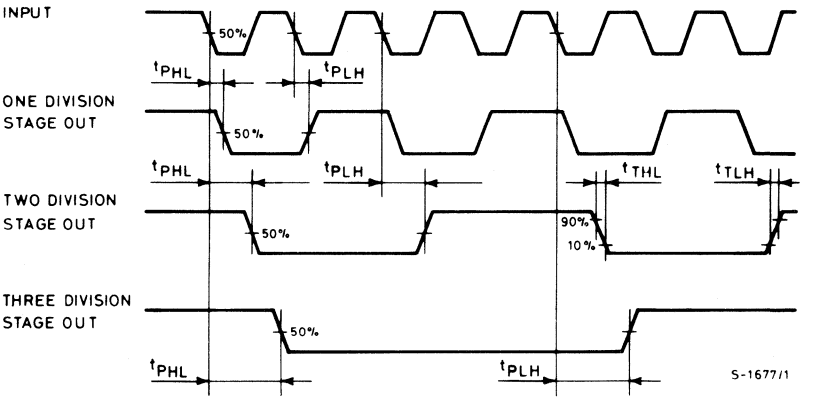
With the exception of V_{O1}, the output where the 10 kHz signal is greatest is V_{OX}.
This operation is repeated for all the inputs.

TIMING DIAGRAM

For M740/M747



For M738/M741



COS/MOS INTEGRATED CIRCUIT

M 750

PRELIMINARY DATA

23 STAGE COUNTER WITH INTERMEDIATE OUTPUT AT THE 16th STAGE

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 17V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY FOR CRYSTAL OSCILLATOR TIMING APPLICATION
- ADJUSTABLE FREQUENCY DIVIDER IN 127 STEPS
- TEST OUTPUT AVAILABLE
- MOTOR DRIVE BRIDGE CONFIGURATION OUTPUT

The M750 is a 23 stage binary counter in COS/MOS technology in a single monolithic chip. An inverter is available for crystal oscillator application in which the function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose seven adjustment terminals are provided on the M750: they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 16. If one or more adjustment terminals are grounded (taken to pin 14), the output frequency decreases. With an oscillator frequency of 4.194812 MHz the bridge configuration outputs supply two symmetrical square wave signals whose frequency is 0.5 Hz; the pulse duty factor is 0.5 and their relative delay is of half period. The intermediate output provides a 64 Hz signal with pulse duty cycle of 50%. The by-four-divided oscillator frequency may be checked at a separate test output (pin 9) non-reactive with respect to the oscillator. The device is available in 16 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.3 to +17	V
I_{12}, I_{13}	Output current	30	mA
P_{tot}	Power dissipation at T_{amb} = 25°C	200	mW
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +125	°C

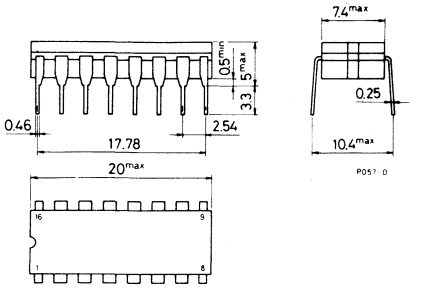
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages values are refered to V_{SS} pin voltage.

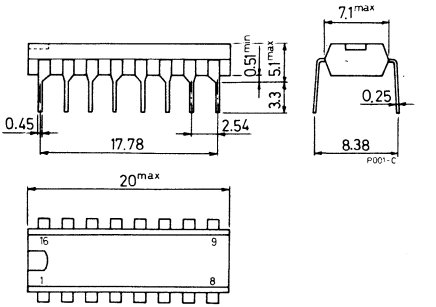
ORDERING NUMBERS: M750 B1 for dual in-line plastic package
M750 D1 for dual in-line ceramic package frit seal

MECHANICAL DATA (dimension in mm)

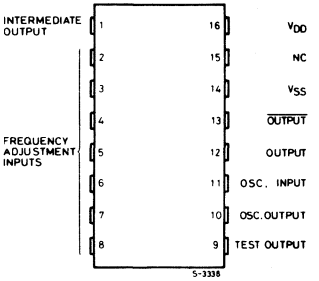
For dual in-line ceramic package, frit seal



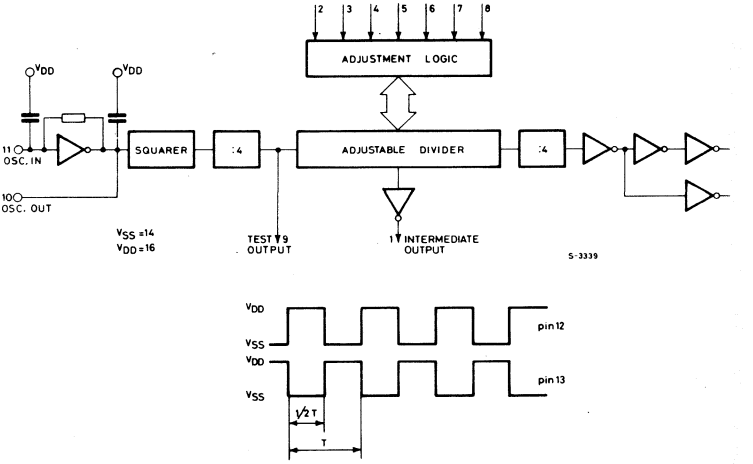
For dual in-line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM and OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 16.5	V
	for oscillator starting	6 to 16.5	V
V_i	Input voltage	V_{DD} to V_{SS}	V
R_L	Output load resistance between pin 12 and 13	300	Ω
T_{op}	Operating temperature	-40 to +85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output high voltage	$I_{OH}=0$		6	5.99			5.99	6		5.95			V
				12	11.99			11.99	12		11.95			
V_{OL}	Output low voltage	$I_{OL}=0$		6			0.01		0	0.01			0.05	V
				12			0.01		0	0.01			0.05	
I_{DN}	Output drive current N-chan.	pin 12-13	2	6	10.5			10	12.5		6.5			mA
			2	12	17			16.5	20		6.5			
I_{DP}	Output drive current P-chan.	pin 12-13	4	6	-10.5			-10	-12.5		-6.5			mA
			10	12	-17			-16.5	-20		-6.5			
I_{ON}	Current consumption	$I_O=0$*		12					3					mA

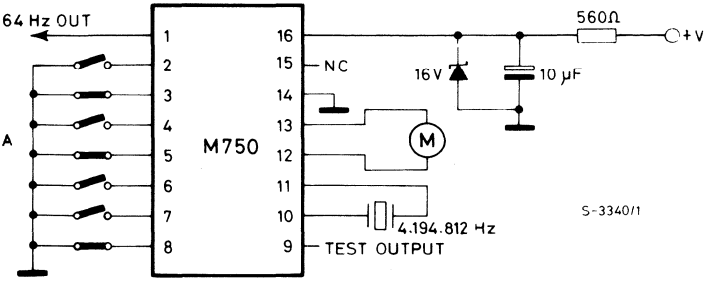
* At quartz frequency of 4.194.812 Hz.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, quartz frequency 4.194.812 Hz)

Parameter		Test conditions		Values						Unit
			V_{DD} (V)	M750 D1			M750 B1			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
f_T	Frequency test output		12		1.048703			1.048703		Hz
f_o**	Output frequency		12		0.5			0.5		Hz
$\frac{\Delta f_o}{f_o}$	Range output frequency adjustment		12		± 121			± 121		ppm
R_o	Total bridge output resistance	$R_L=300\Omega$	6			300			300	Ω

** At the centre position of the variable divider.

APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUIT

M 751

PRELIMINARY DATA

DUAL TONE MULTIFREQUENCY GENERATOR

- 2.5 TO 5V SUPPLY RANGE
- VERY LOW POWER CONSUMPTION
- INTERNAL PULL-UP RESISTOR WITH DIODE PROTECTION ON ALL KEYBOARD INPUTS
- ON-CHIP CRYSTAL CONTROLLED OSCILLATOR (f_o = 4.433619 MHz) WITH INTEGRATED FEEDBACK RESISTOR AND LOAD CAPACITORS
- LOW HARMONIC DISTORTION
- FIXED PRE-EMPHASIS ON HIGH-GROUP TONES
- FAST START-UP TIME

The M751 provides all the tone frequency pairs required for a DTMF Dialling System. Tones are obtained from an inexpensive TV crystal (f_o= 4.433619 MHz) followed by two independent programmable dividers. The dividing ratio is controlled by the selected key. Keyboard format is 4 rows x 4 columns and a key is valid when a column and a row are simultaneously grounded. Internal logic prevents the transmission of illegal tones when more than one key is pressed. Individual tones can be obtained grounding the corresponding row of column input. D/A conversion is accomplished by a capacitive network allowing very low power consumption, very low distortion and an exceptional stability of tone level against temtemperature variations. The tones are mixed in a resistive network; a unity gain amplifier is provided to realize a two pole active filter with only four external passive components. SGS-ATES has also developed the LS342, DTMF line interface, which provides the stabilized supply for the M751 from the telephone line and amplifiers the output tones to the standardized levels. The M751 utilizes low voltage COS/MOS technology and is available in 16 pin dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.5 to +5.5	V
V_I	Input voltage	-0.3 to V_{DD} +0.5	V
P_{tot}	Power dissipation	400	mW
T_{op}	Operating temperature range	-25 to +50	°C
T_{stg}	Storage temperature range	-25 to +125	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

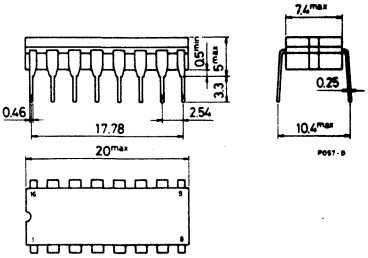
** All voltages are referred to V_{SS} pin voltage.

ORDERING NUMBERS: M751 B1 for dual in-line plastic package
M751 F1 for dual in-line ceramic package (frit seal)

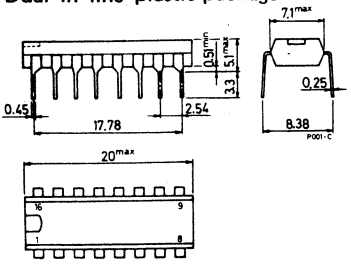
M 751

MECHANICAL DATA (dimensions in mm)

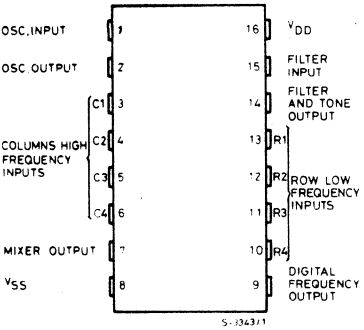
Dual in-line ceramic package, frit seal)

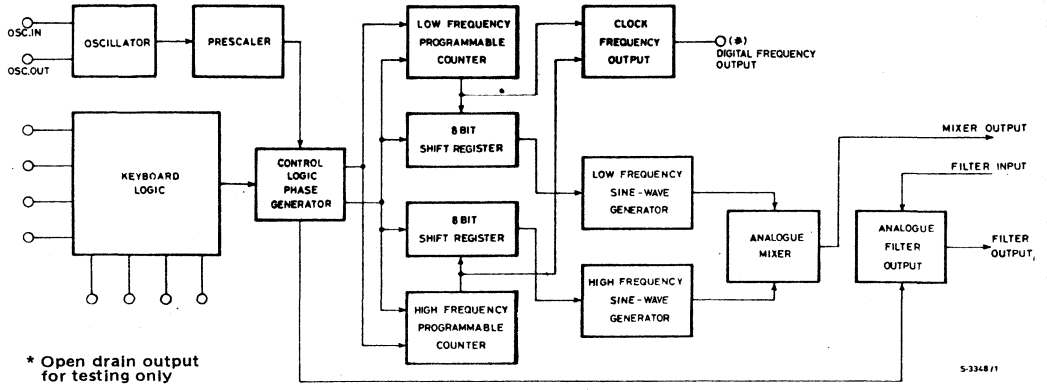


Dual in-line plastic package



PIN CONNECTIONS





ELECTRICAL CHARACTERISTICS (All parameters are tested at T_{amb}= 25°C)

	Parameter		Test conditions (see note 1)	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS							
Supply	V_{DD}	Voltage supply range		2.5	3	5	V
	I_{DD}	Operating supply current	V_{DD}= 2.5V			2	mA
Row and column inputs	I_{IH}	High level input current	V_{DD}= 3V V_{IH}= 3V			1	μA
	I_{IL}	Low level input current	V_{DD}= 3V V_{IL}= 0V		-60	-80	μA
	V_{IH}	High level input voltage		0.7V_{DD}			V
	V_{IL}	Low Level input voltage				0.3V_{DD}	V
Oscillator	I_{IH}	High level input current	V_{DD}= 3V V_{IH}= 3V			1	μA
	I_{IL}	Low level input current	V_{DD}= 3V V_{IL}= 0V			1	μA
	I_{OH}	High level output current	V_{DD}= 2.5V V_{OH}= 2V	-300	-500		μA
	I_{OL}	Low level output current	V_{DD}= 2.5V V_{OL}= 0.5V	300	500		μA
Digital freq. output	I_{OL}	Low level output current (open drain output)	V_{DD}= 3V V_{OL}= 1V	200			μA
Filter	V_O	Output DC voltage without tones	V_{DD}= 2.5V			200	mV
	V_O	Output DC voltage with 2 tones	V_{DD}= 2.5V (see fig. 1) (see note 2)	0.81	0.84	0.87	V
Oscillator	R_F	Feedback oscillator resistance		4	4.5		MΩ
	C_I	Input capacitance to V_{DD}			9.5	10.5	pF
	C_O	Output capacitance to V_{DD}			10.5	11.5	pF
Mixer	Z_{O1}	Output dynamic impedance with 2 tones	V_{DD}= 2.5V		10		kΩ
Filter	Z_{O2}	Output dynamic impedance with 2 tones	V_{DD}= 2.5V		2.5		kΩ
Tone characteristics	$\frac{\Delta F}{F}$	Max. output tone deviation from standard	At crystal frequency f_o= 4.433619 MHz				
		R_1 697 Hz				+0.5	%
		R_2 770 Hz				-0.2	%
		R_3 852 Hz				+0.5	%
		R_4 941 Hz				-0.6	%
		C_1 1209 Hz				+0.6	%
		C_2 1336 Hz				-0.4	%
		C_3 1477 Hz				-0.3	%
		C_4 1633 Hz				+1.1	%

ELECTRICAL CHARACTERISTICS (continued)

		Parameter	Test conditions (see note 1)	Min.	Typ.	Max.	Unit
Tone characteristics	V_{LF}	Low frequency tones amplitude at pin 14	V_{DD}= 2.5V (see fig. 2) (see fig. 3) (see note 3)	150	175	200	mVpp
	V_{HF}	High frequency tones amplitude at pin 14		195	220	245	mVpp
		Pre-emphasis		1	2	3	dB
		Unwanted frequency components at f = 3.4 kHz at f = 50 kHz				-33 -80	dBm dBm
		Total harmonis distortion for a single frequency	V_{DD}= 2.5V (see fig. 3)			2	%
	t_s	Start up time	V_{DD}= 2.5V (see fig. 4) (see fig. 5)		3	5	ms
	t_r	Supply voltage rise time	V_{DD}= 2.5V			250	ms

Note 1: This device has been designed to be connected to LS342 MF tone dialler line interface, from which it takes a V_{DD}= 2.5V min. therefore many parameters are tested at this value.

Note 2 : The value of DC output component at two different conditions of supply voltages, with two tones activated, can be related as follows:

$$V_{DC'} = V_{DC} \frac{V_{DD'}}{V_{DD}}$$

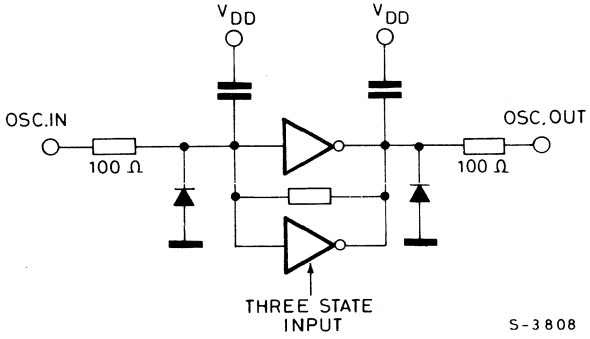
Note 3 : The value of AC output components (V_{LF}, V_{HF}) at two different conditions of supply voltages can be related as follows:

$$V_{LF'} = V_{LF} \frac{V_{DD'}}{V_{DD}} \qquad V_{HF'} = V_{HF} \frac{V_{DD'}}{V_{DD}}$$

FUNCTIONAL DESCRIPTION

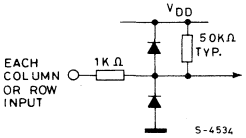
Oscillator (OSC. IN pin 1 – OSC. OUT pin 2)

The oscillator circuit has been designed to work with a 4.433619 MHz crystal ensuring both fast start-up time and low current consumption.
When V_{DD} is applied and a key is activated two inverters are paralleled (see figure below) to decrease the total r_{on} resistance.
After oscillations have started one of the two buffers is switched off and the current consumption is reduced to 2/3 of the initial value.
Feedback resistance and load capacitances are integrated on the chip ensuring good temperature performance.



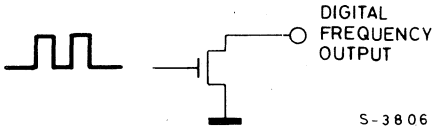
Keyboard inputs (Columns: pins 3 – 6 – Rows: pins 10 – 13)

Each input has a protection circuit and a pull-up resistance (see fig. below).
If only one of these inputs is grounded a single tone will appear at the output.
If a column and a row input are grounded two tones will appear at the output.
If two inputs of the same group are grounded no tones will be generated.



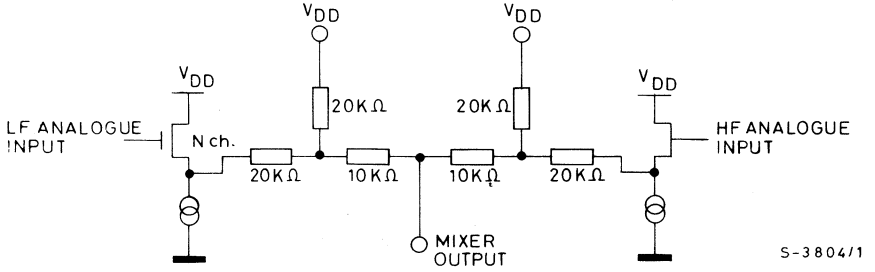
Digital frequency output (pin 9)

This output is intended for testing only; when a single tone is activated, at this output is available a digital signal whose frequency is 16 times the selected output tone frequency. This output is an open collector N-channel transistor.



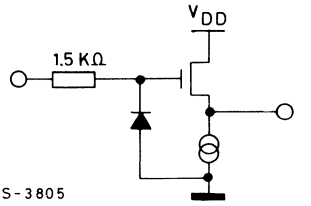
Mixer output (pin 7)

The two reconstructed sine waves are buffered then mixed in a resistive array network that also restores the DC output level.

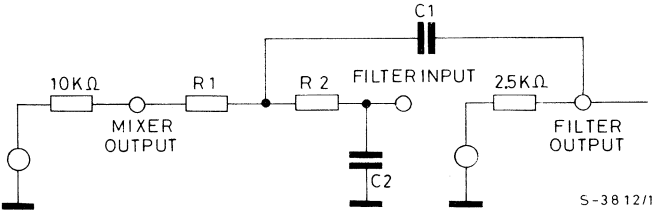


Filter (Filter input pin 15, Filter output pin 14)

A unity gain amplifier is available to realize a two pole active filter (see fig. below).
The output of this amplifier is held low until tones are valid, it than rises to about 0.85V at V_{DD}= 2.5V. Tone are superimposed on this DC.
The output DC component is very precise and stable to allow DC coupling with the LS342 DTMF line interface.



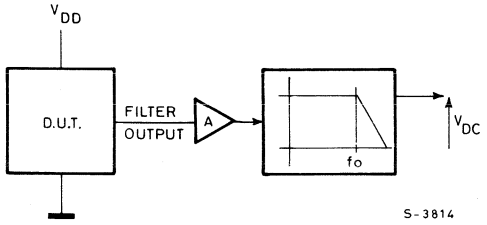
The output dynamic impedance of the filter is about 2.5 kΩ.
The following equivalent circuit should be applied during filter design:



It is evident that R_1 and R_2 should be kept high to avoid undue influence of Mixer and Filter output impedances.
The following values are suggested:

R_1= 430 kΩ ± 2% R_2= 82 kΩ ± 2% C_1= 820 pF ± 10% C_2= 120 pF ± 10%

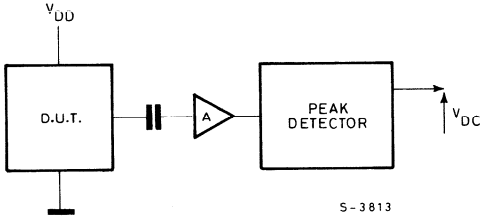
Fig. 1 - DC filter output level measurement test set.



Low pass filter characteristics:
f_o = 100 Hz 40 dB/dec

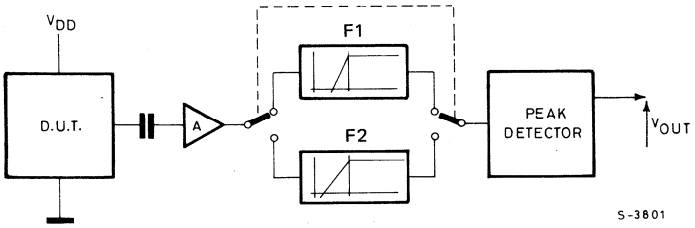
This measurements is performed with only one tone available at the output.

Fig. 2 - Output tone level measurement test set.



This measurement is performed with one tone present at the output.

Fig. 3 - THD measurement test set.



High pass filter characteristics:
F1: f_o= 1400 Hz 100 dB/dec
F2: f_o= 2500 Hz 100 dB/dec

THD measurement is made sensing the level of harmonic components after suppression of the fundamental. Two different high pass filters are used for low and high frequency tones.

Fig. 4 - Start-up time measurement test set

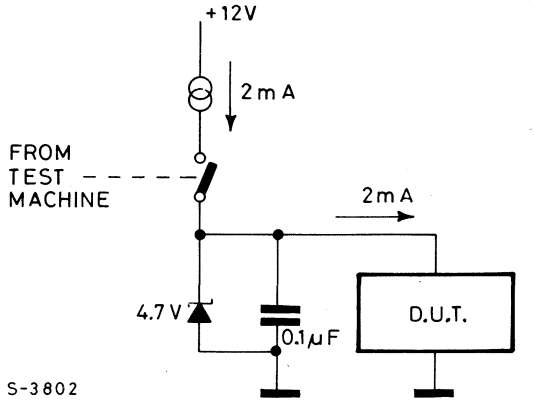
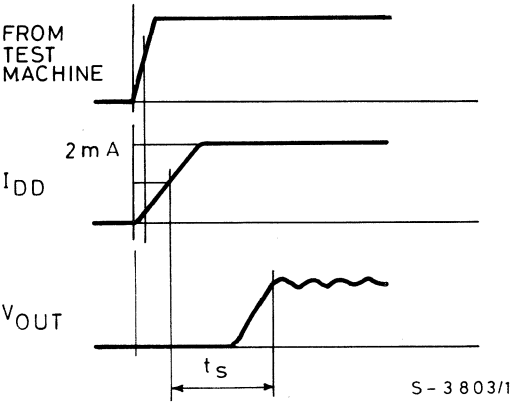
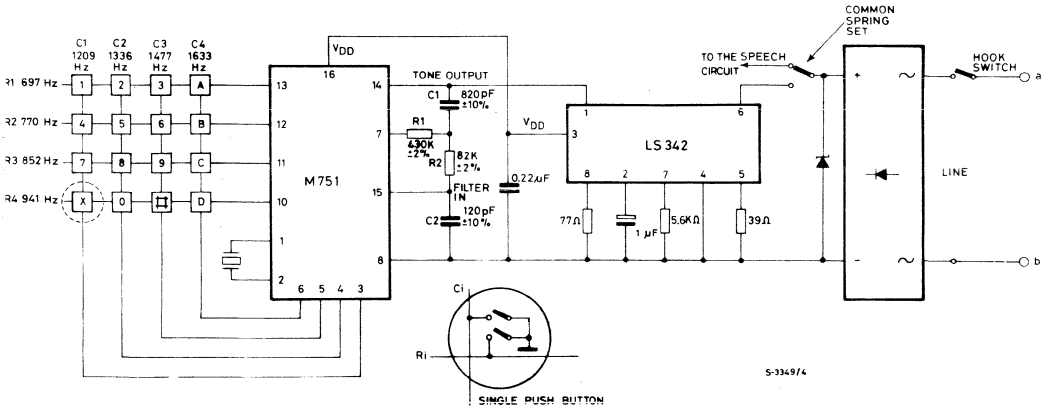


Fig. 5 - Start-up time definition



APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUIT

M 752

PRELIMINARY DATA

16 STAGE COUNTER

- LOW QUIESCENT POWER DISSIPATION
- WIDE SUPPLY VOLTAGE RANGE: 3 to 17V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY FOR CRYSTAL OSCILLATOR TIMING APPLICATION
- ADJUSTABLE FREQUENCY DIVIDER IN 127 STEPS
- TEST OUTPUT AVAILABEL
- MOTOR DRIVE BRIDGE CONFIGURATION OUTPUT

The M752 (standard temperature range) is a 16 stage binary counter in COS/MOS technology in a single monolithic chip. An inverter is available for crystal oscillator application in which the function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose seven adjustment terminals are provided on the M752: they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. With an oscillator frequency of 4.194812 MHz the bridge configuration outputs supply two symmetrical square wave signals whose frequency is 64 Hz; duty cycle is 50% and their relative delay is of half period. The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 16. If one or more adjustment terminals are grounded (taken to pin 14), the output frequency decreases. If all adjustment terminals are grounded, the output frequency is reduced by 242 ppm. The by-four-divided oscillator frequency may be checked at a separate test output (pin 9) non-reactive with respect to the oscillator. Based on this check the output frequency and consequently the accuracy of the clock may be adjustable at the terminals 2 . . . 8 by means of the variable frequency divider. The device is available in 16 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.3 to +17	V
I_{12}, I_{13}	Output current	30	mA
P_{tot}	Power dissipation at $T_{amb} = 25°C$	200	mW
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +125	°C

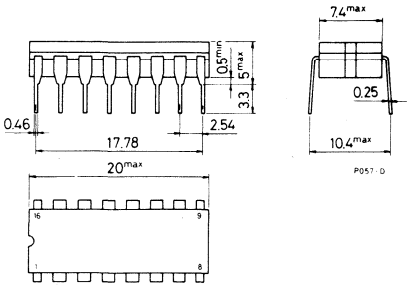
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are referred to V_{SS} pin voltage.

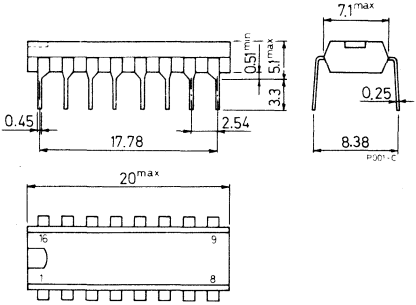
ORDERING NUMBERS: M752 B1 for dual in-line plastic package
M752 D1 for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimension in mm)

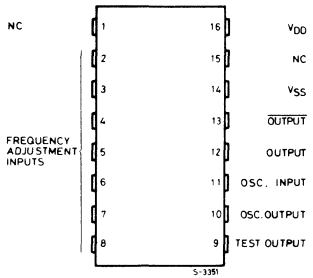
For dual in-line ceramic package, frit seal



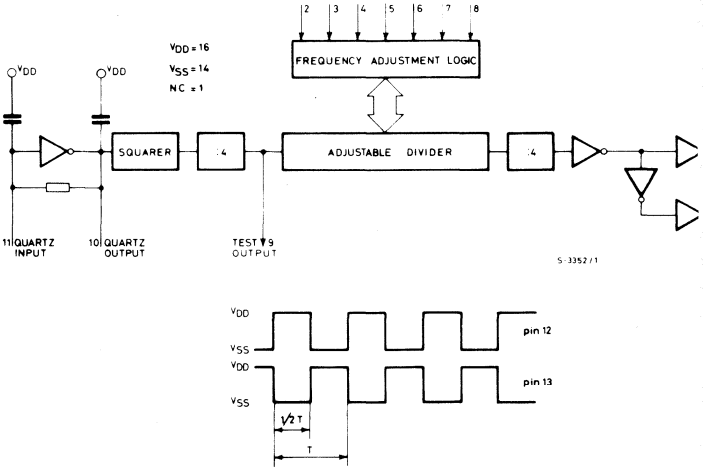
For dual in-line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM and OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 16.5	V
V_{DD}	for oscillator starting	6 to 16.5	V
V_i	Input voltage	V_{DD} to V_{SS}	V
R_L	Output load resistance between pins 12 and 13	1	KΩ
T_{op}	Operating temperature	-40 to +85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions			Values									Unit
			V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output high voltage	I_{OH}= 0		6	5.99			5.99	6		5.95			V
				12	11.99			11.99	12		11.95			
V_{OL}	Output low voltage	I_{OL}= 0		6			0.01		0	0.01			0.05	V
				12			0.01		0	0.01			0.05	
I_{DN}	Output drive current N-channel	pin 12-13	2	6	10.5			10	12.5		6.5			mA
			2	12	17			16.5	20		6.5			
I_{DP}	Output drive current P-channel	pin 12-13	4	6	-10.5			-10	-12.5		-6.5			mA
			10	12	-17			-16.5	-20		-6.5			
I_{ON}	Current consumption	I_O= 0*		12					3					mA

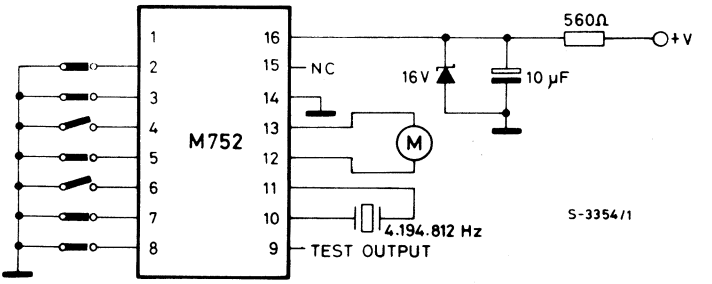
* At quartz frequency of 4.194.812 Hz.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, quartz frequency 4.194.812 Hz)

Parameter		Test conditions	V_{DD} (V)	Values						Unit
				M752 D1			M752 B1			
				Min.	Typ.	Max.	Min.	Typ.	Max.	
f_T	Frequency test output		12		1.048703			1.048703		Hz
f_o **	Output frequency		12		64			64		Hz
$\frac{\Delta f_o}{f_o}$	Range output frequency adjustment		12		± 121			± 121		ppm
R_o	Total bridge output resistance	R_L= 300Ω	6			300			300	Ω

** At the centre position of the variable divider.

APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUIT

M 754

PRELIMINARY DATA

23 STAGE COUNTER WITH INTERMEDIATE OUTPUT AT THE 16th STAGE

- LOW QUIESCENT POWER DISSIPATION
- 25% OUTPUT PULSE DUTY CYCLE
- WIDE SUPPLY VOLTAGE RANGE: 3 to 17V
- FULLY PROTECTED INPUTS
- INVERTER AVAILABILITY FOR CRYSTAL OSCILLATOR TIMING APPLICATION
- ADJUSTABLE FREQUENCY DIVIDER IN 127 STEPS
- TEST OUTPUT AVAILABLE
- MOTOR DRIVER BRIDGE CONFIGURATION OUTPUT

The M754 (standard temperature range) is a 23 stage binary counter in COS/MOS technology in a single monolithic chip. An inverter is available for crystal oscillator application in which the function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose seven adjustment terminals are provided on the M754; they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 16. If one or more adjustment terminals are grounded (taken to pin 14), the output frequency decreases. With an oscillator frequency of 4.194812 MHz the bridge configuration outputs supply two square wave signals whose frequency is 0.5 Hz; the pulse duty factor is 0.25 and their relative delay is of half period. The intermediate output provides a 64 Hz signal with pulse duty cycle of 50%. The by-four-divider oscillator frequency may be checked at a separate test output (pin 9) non-reactive with respect to the oscillator. The device is available in 16 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.3 to +17	V
I_{12}, I_{13}	Output current	30	mA
P_{tot}	Power dissipation at T_{amb}= 25°C	200	mW
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +125	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

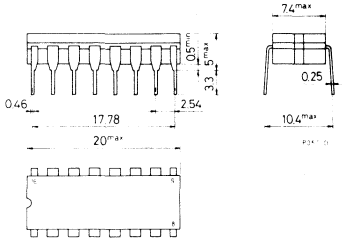
** All voltages are referred to V_{SS} pin voltage.

ORDERING NUMBERS: M754 B1 for dual in-line plastic package
M754 D1 for dual in-line ceramic package frit seal

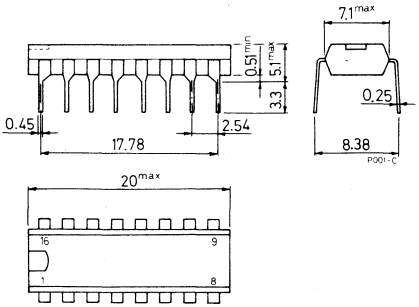
M 754

MECHANICAL DATA (dimension in mm)

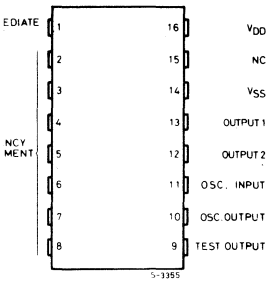
For dual in-line ceramic package, frit seal



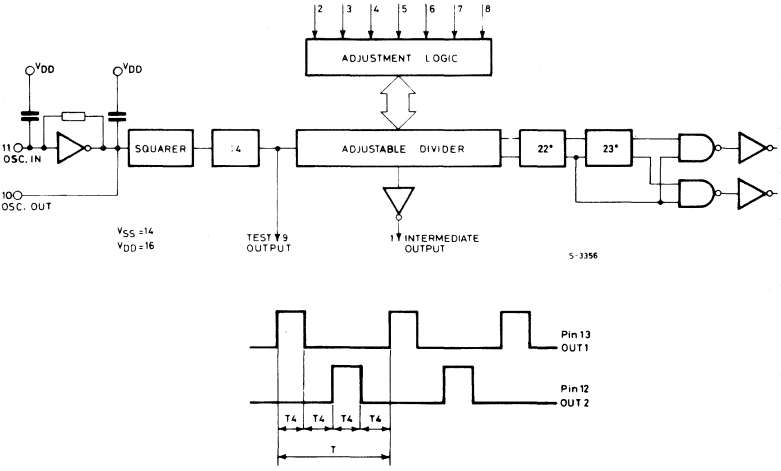
For dual in--line plastic package



PIN CONNECTIONS



BLOCK DIAGRAM and OUTPUT WAVEFORM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: for general applications	3 to 16.5	V
	for oscillator starting	6 to 16.5	V
V_i	Input voltage	V_{DD} to V_{SS}	V
R_L	Output load resistance between pins 12 and 13	300	Ω
T_{op}	Operating temperature range	-40 to +85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions	V_O (V)	V_{DD} (V)	Values -40° C Min.	-40° C Typ.	-40° C Max.	25° C Min.	25° C Typ.	25° C Max.	85° C Min.	85° C Typ.	85° C Max.	Unit
V_{OH}	Output high voltage	I_{OH}= 0		6	5.99			5.99	6		5.95			V
				12	11.99			11.99	12		11.95			
V_{OL}	Output low voltage	I_{OL}= 0		6			0.01		0	0.01			0.05	V
				12			0.01		0	0.01			0.05	
I_{DN}	Output drive current P-channel	pin 12-13	2	6	10.5			10	12.5		6.5			mA
			2	12	17			16.5	20		6.5			
I_{DP}	Output drive current N-channel	pin 12-13	4	6	-10.5			-10	-12.5		-6.5			mA
			10	12	-17			-16.5	-20		-6.5			
I_{ON}	Current consumption	I_O= 0*		12					3					mA

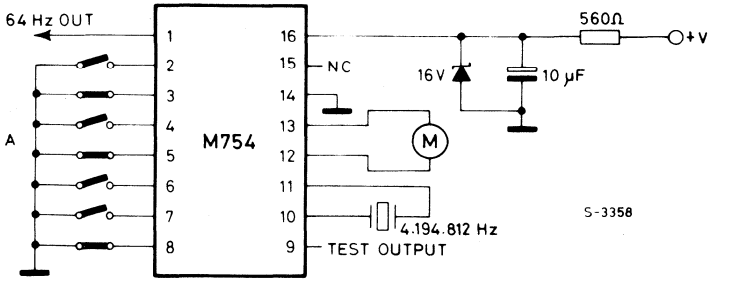
* At quartz frequency of 4.194.812 Hz.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, quartz frequency 4.194.812 Hz)

Parameter		Test conditions	V_{DD} (V)	Values M754 D1 Min.	M754 D1 Typ.	M754 D1 Max.	M754 B1 Min.	M754 B1 Typ.	M754 B1 Max.	Unit
f_T	Frequency test output		12	1.048703			1.048703			Hz
f_o**	Output frequency		12		0.5			0.5		Hz
$\frac{\Delta f_o}{f_o}$	Range output frequency adjustment		12		± 121			± 121		ppm
R_o	Total bridge output resistance	R_L= 300Ω	6			300			300	Ω

** At the centre position of the variable divider.

APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUITS

M 755
M 756

PRELIMINARY DATA

CLOCK/DISPLAY INTERFACE FOR MICROPROCESSORS

- DAY, HOUR AND MINUTE COUNT
- 1 Hz FLASHING COLON
- 24 HOUR (M755) or 12 HOUR (M756) MODES
- INTERNAL OSCILLATOR (32.768 KHz)
- OVERFLOW OUTPUT
- BCD MULTIPLEXED OUTPUTS FOR STANDARD 7-SEGMENT DECODER/DRIVER
- DISPLAY OF TIME OR OF DATA REGISTERS
- MICROPROCESSOR CONTROLLED DECIMAL POINT

The M755 and M756 are COS/MOS clocks specially designed for battery backed up applications in Microprocessor based systems. The circuits include also a day of the week count section.
The content of the counters can be read by the Microprocessor and/or displayed using a standard BCD to 7-segment LED decoder driver.
The circuits also provide a 1 Hz flashing colon output.
It is possible to display the content of the data registers instead of the clock section output to show, for instance, the TV channel and program number.
The same registers can be used as a 5 x 4 non-volatile memory.
The M755 and M756 interface with a Microprocessor I/O port by a 4 bit bidirectional bus and two strobe signals which are used to address, load and read the internal registers and counters.
The circuits are produced using a Low-Voltage COS/MOS technology and are assembled in 24-lead dual in-line plastic or ceramic frit seal packages.

ABSOLUTE MAXIMUM RATING*

V_{DD} **	Supply voltage	-0.3 to 6 V
V_I	Input voltage	-0.3 to V_{DD} +0.3 V
I_I	DC input current	± 1 mA
$V_{o(off)}$	Off-state output voltage	6 V
I_{OH}	Continuous output source current DP, PM outputs	-25 mA
	D1 to D4 outputs	-10 mA
P_{tot}	Total power dissipation (per package)	300 mW
	Dissipation per output transistor	100 mW
T_{op}	Operating temperature range	0 to 70 °C
T_{stg}	Storage temperature range	-65 to 150 °C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

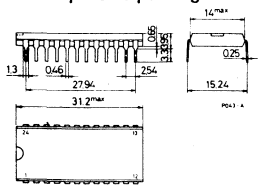
** All voltages are with respect to V_{SS} (GND).

ORDERING NUMBERS: M755 B1 for dual in-line plastic package
M756 B1 for dual in-line plastic package
M755 F1 for dual in-line ceramic frit seal package
M756 F1 for dual in-line ceramic frit seal package

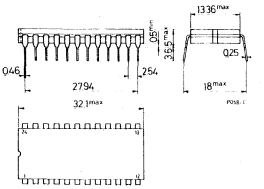
M 755
M 756

MECHANICAL DATA (dimension in mm)

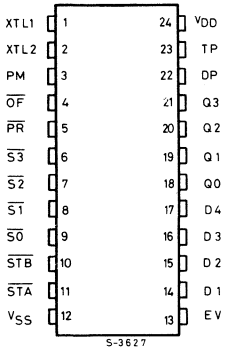
Dual in-line plastic package



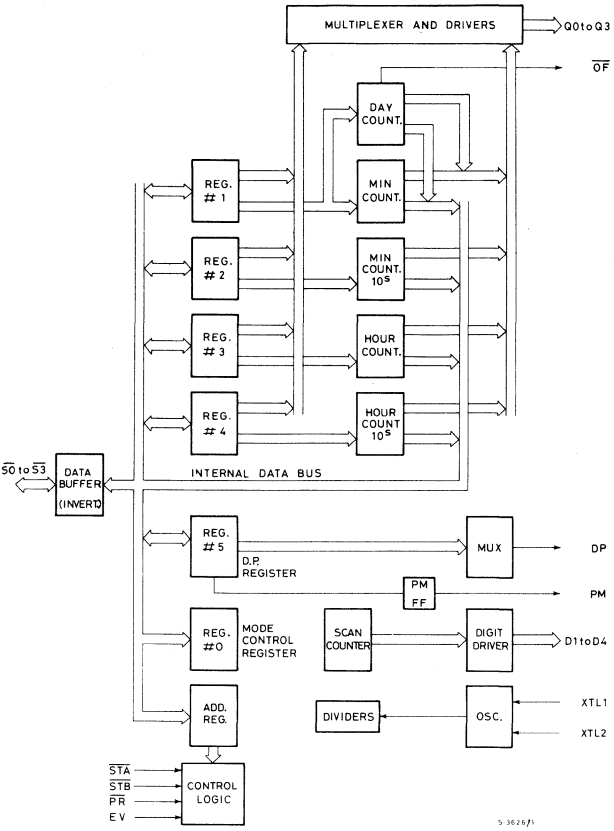
Dual in-line ceramic frit seal package



PIN CONNECTIONS



BLOCK DIAGRAM



PIN DESCRIPTION

PIN NAME	FUNCTION	NOTE
$\overline{S0}$ to $\overline{S3}$	Data/address bus (4 bits)	Bidirectional, open drain outputs
$\overline{STA}$	Address strobe	Input
$\overline{STB}$	Data strobe	Input
XTL1, XTL2	Crystal connections	XTL1 osc. in, XTL2 osc. out.
D1 to D4	Digit strobes	Outputs, emitter follower
Q0 to Q3	BCD data display	Outputs
DP	Decimal point/flashing colon	Output, emitter follower
PM	PM indication	Output, emitter follower
$\overline{OF}$	Overflow	Output, open drain
$\overline{PR}$	Load counter	Input
EV	External voltage indication	Input
TP	Test pin	Input/output. Leave open circuit

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	2 to 5.25	V
V_I	Input voltage	0 to V_{DD}	V
$V_{O(off)}$	Off-state output voltage	max. 5.25	V
I_{OH}	Pulsed output current DP, PM outputs	max. -20	mA
	D1 to D4 outputs	max. -7	mA
T_{op}	Operating temperature	0 to 70	°C

STATIC ELECTRICAL CHARACTERISTICS

(Over recommended operating conditions, V_{DD}= 5V, unless otherwise specified) Typ. values are at T_{amb}= 25°C

Parameter			Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	All inputs		2.6			V
V_{IL}	Input low voltage	All inputs				0.8	V
I_I	Input leakage current	All inputs	V_I = 0 to 5.25V			10	μA
V_{OL}	Output low voltage	Q0 to Q3 S0 to S3	I_{OL}= 1.6 mA			0.4	V
		D1 to D4 DP, PM	I_{OL}= 40 μA			0.5	
V_{OH}	Output high voltage	DP, PM	I_{OH}= 0	4.25	4.5		V
			I_{OH}= -20 mA	3	4		
		D1 to D4	I_{OH}= 0	4.5	4.75		
			I_{OH}= -7 mA	2	4		
		Q0 to Q3	I_{OH}= -40 μA	3.5	3.75		
I_{DD}	Supply current		V_{DD}= 2.5V (EV input grounded)		15	30	μA
			V_{DD}= 5.25V (all out. and inp. open)		0.5	1	mA

DYNAMIC ELECTRICAL CHARACTERISTICS

(V_{DD}= 5V, T_{amb}= 25°C, C_L= 15 pF at each output)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{w1}	Digit display time	see fig. 1		1.5		ms
t_{w2}	Interval between two digits			0.5		ms
t_{p1}	Propagation delay time				100	ns
t_w	$\overline{STA}$ and $\overline{STB}$ width	see fig. 2, 3	500			ns
t_{h1}	Hold time of $\overline{S0}$ to $\overline{S3}$ from $\overline{STA}$ or $\overline{STB}$	see fig. 2	250			ns
t_{setup}	Set up time of $\overline{STA}$ from $\overline{STB}$		800			ns
t_{h2}	Hold time of $\overline{STA}$ from $\overline{STB}$	see fig. 3	500			ns
t_r	Release time of DATA out from $\overline{STB}$		250			ns

Fig. 1 - Display timing

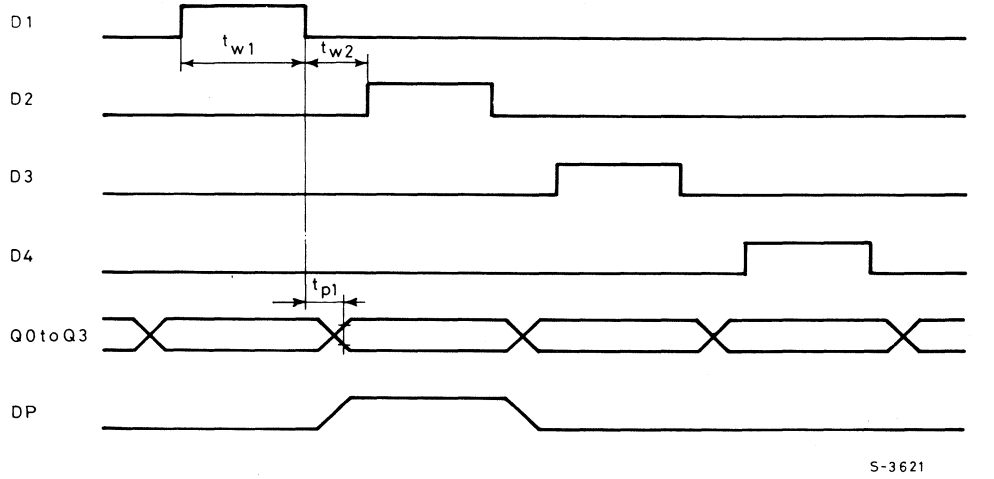


Fig. 2 - Write timing

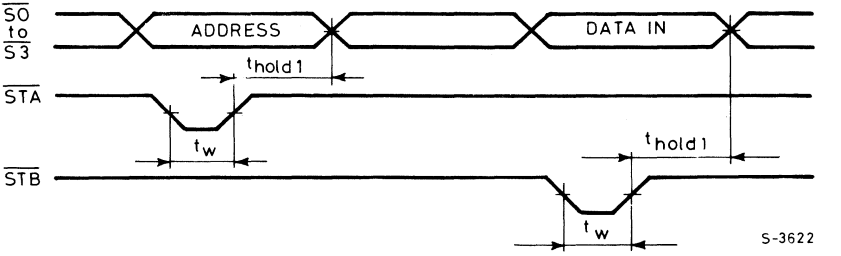
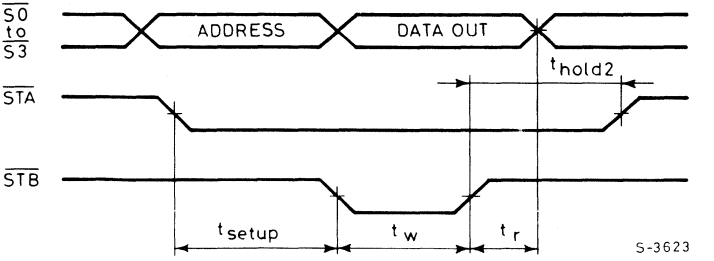


Fig. 3 - Read timing



DESCRIPTION

Data Buffer

This bidirectional, open drain, four bit data buffer is used to interface the M755/6 with the Microprocessor. Data is transmitted or received by the buffer and also Control words and Address are received through it. Note that this buffer is inverting and the I/O lines are not provided with pull-up.

Control Logic

The function of this block is to manage all the internal and external Data transfers.
This block in controlled by Data and Address Strobes ($\overline{STA}$ and $\overline{STB}$), by two other inputs ($\overline{PR}$ and EV) and in turn generates the operation as described in table 1.
The source or the destination of data depends on the contents of the Address Register and Control Register.

Table 1 - Truth table of the control logic block

EV	$\overline{PR}$	$\overline{STA}$	$\overline{STB}$	OPERATION
L	H	X	X	Outputs off, all inputs disabled
H	H	H	H	Data Buffer High impedance
H	H	L	H	Address Register loading
H	H	H	L	Data loading in the selected register
H	H	L	L	Reading back of the selected register or counter
H	L	X	X	Counters loading from registers 1 to 5, count off
H	⌐	X	X	Normal operation

Address Register

The function of this register is to latch the address of the register involved on the actual I/O cycle. Therefore it must be loaded at the start of any I/O cycle.
It is possible to address six registers: a 0 in this register always addresses the Mode Control Register and a BCD 5 addresses the D.P. Register, independently of the content of the Mode Control Register.
The BCD figure from 1 to 4 can address many registers, in conjunction with the content of the Mode Control Register.

Mode Control Register

This register selects the operating mode in order to select the group of counters or registers that must be read, displayed or loaded.
Table 2 shows the function that can be selected.

Table 2 - Truth table of the Mode Control Register

Mode number	Control word				Function
	$\overline{S3}$	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	
0	X	H	H	H	Set Register out (Read and Display)
1	X	H	H	L	Set Clock Counters out (Read and Display)
2	X	H	L	H	Day Counter out (Read and Display)
3	X	H	L	L	Load Clock Counter and PM
4	X	L	H	H	Load Day Counter
5	X	L	H	L	Don't care
6	X	L	L	H	Don't care
7	X	L	L	L	Don't care (see note 1)

Note 1: This configuration must be used for a very low power consumption during battery back-up.

Mode 0-Set Registers read/display
When programmed, this mode enables the content of Register 1 to 4 to be displayed or read back through the Data Buffer.
This mode resets automatically the Mode 1, if previously programmed.

Mode 1-Set Clock Counters read/display
When programmed, this mode enables the content of Clock Counters to be displayed or read back through the Data Buffer. This mode resets the Mode 0, if previously programmed.

Table 3 - Counters Selection (Read)

Address	Counter
1	Minutes
2	10's of minutes
3	Hours
4	10's of hours

Mode 2-Day Counter read/display
When selected, this mode enables the content of the Day Counter to be displayed or read back through the Data Buffer. This mode is active only if Mode 1 was previously programmed.
The content of the Day Counter is displayed during the digit 1 time and can be read back as register 1.

Mode 3-Load Clock Counters and PM
This mode enables the loading of Data from Registers 1 to 5 into the clock counters and PM flip-flop. This can also be done by connecting the $\overline{PR}$ input Low.

Table 4 - Register to Counter transfer

Register	Counter
1	Minutes
2	10's of minutes
3	Hours
4	10's of hours

Table 5 - PM flip-flop, Set/Reset table

Register-5	PM
0	Set
any	Reset

Mode 4-Load Day Counter
This mode enables the loading of register 1 into the Day counter.
All other counters are unaffected.

D.P. Register, output

The function of this register is to latch the value of decimal point output D.P. for any of the four digits. A bit "1" turns on the D.P. output, a "0" turns it off.

Table 6 - D.P. (Register 5)

3	2	1	0	Bit number
4	3	2	1	Digit
10's hour	hour	10's min.	min.	

When M755/M756 are programmed in Mode 1, the decimal point D.P. is switched at 1 Hz rate, if generated at digits time 3 or 2.
This feature is provided to accomodate displays with right hand D.P., left hand D.P. or with a colon. The output has emitter follower configuration.

Oscillator

An external quartz crystal, resonant a 32 768 KHz, connected at XTL1 and XTL2 pins sets the internal oscillator to the correct input frequency. This frequency is divided and used for both scanning of the display control (500 Hz) and time counting (1 Hz).
An external clock signal may be applied to pin 1 or pin 2 with pin 1 connected to V_{SS} to V_{DD}.

P.M. output

This output is available for P.M. time indication only in 12 hour mode and has emitter follower configuration.
The P.M. status can be read back checking the conditions of the bit number 3 of the 10's of hours counter (1 = P.M., 0 = A.M.).

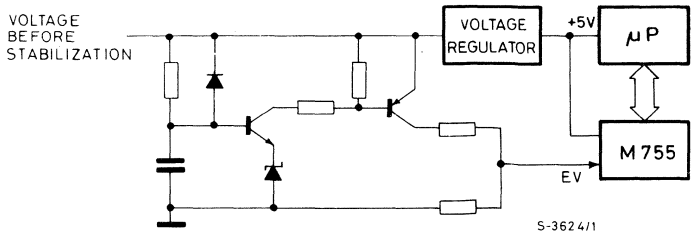
$\overline{OF}$ output

The $\overline{OF}$ output (overflow) has open drain configuration. It goes active (Low) on the 23.59/0.00 transition for 30" (M755) or on PM/AM transition 11.59/12.00 for 60' (M756).

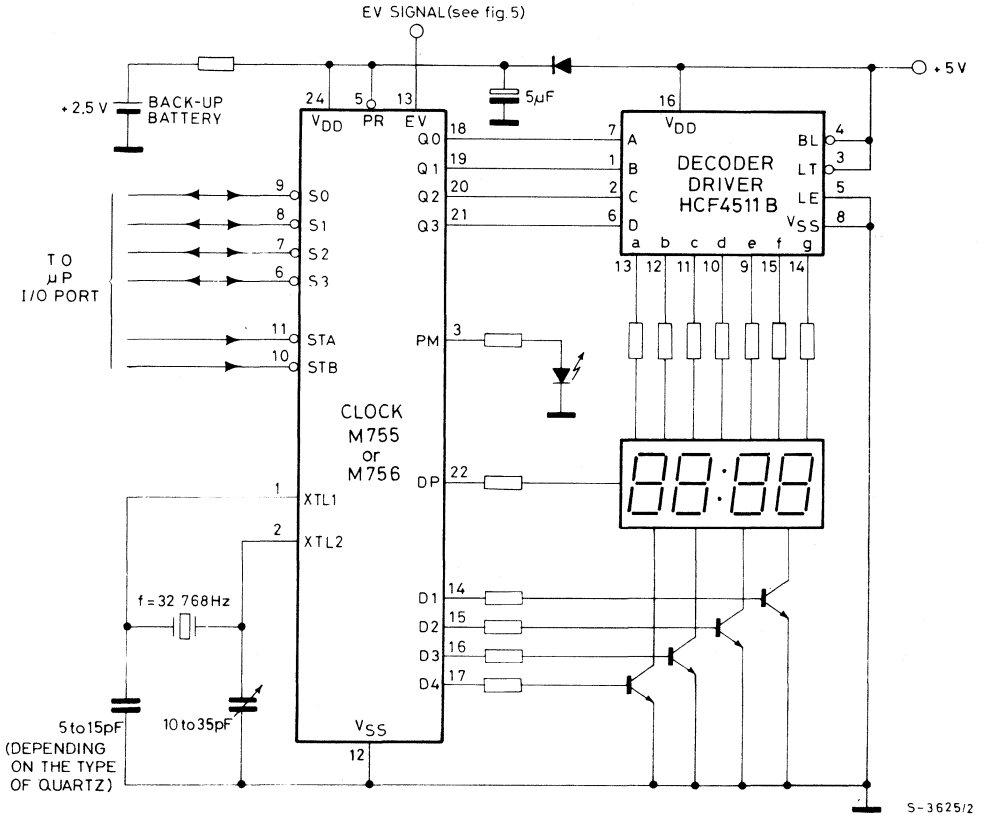
EV input

This EV input (External Voltage) is used during battery powered operation.
In this case, a low level on the EV input switches off all outputs in order to reduce power consumption. In addition, all inputs are disabled in order to prevent affecting of register during power down of the microprocessor which controls the M755/M756.
Figure 5 shows a circuit which could be used to generate EV:

Fig. 5 - EV Signal Generation



APPLICATION CIRCUIT



COS/MOS INTEGRATED CIRCUITS

M 760
M 760A

ADVANCE DATA

LOOP DISCONNECT DIALLER

- DIRECT TELEPHONE LINE OPERATION
- LOW VOLTAGE COS/MOS TECHNOLOGY
- LOW POWER CONSUMPTION IN STAND-BY MODE
- PIN SELECTABLE LONG DISTANCE CALL INHIBITION
- PIN SELECTABLE OUTPUT PULSING INHIBITION
- 8 SELECTABLE ACCESS PAUSES
- WIDE SELECTION OF MASK OPTIONS FOR 1.5-1.6-1.66-2 B/W RATIOS

The M760 Loop Disconnect Dialler provides the features to implement a pulse dialler with redial. It can be operated directly by the telephone line current and convert a single per key contact into the corresponding pulse signals to simulate the rotary dialler.
When in stand-by condition it requires only few microamperes to maintain the storage of the last call. Keyboard inputs are fully static; outputs are provided to pulse the telephone line and to mute the receiver during impulsing.
Other features are: pin selectable long distance call inhibition, 24 digit memory in which can be introduced a maximum of 8 access pauses, pin selectable redial inhibition and out pulsing inhibition for operation with payment-card telephones.
Redial can be achieved with two pin selectable procedures.
The device requires an inexpensive 455 kHz ceramic resonator and is designed to minimize external components.
The unique design of the power-on reset circuit can avoid the need for a special dedicated spring in the hook switch.
The loop is disconnected for a time longer than 300 msec when fraudulent dialling is tried with the hook or any external device by sensing the line condition at the input LS.
The M760 is realized in low voltage COS/MOS technology and can be easily mask programmed to meet all administration standards; it is available in a 24 pin dual in-line plastic or ceramic package; the M760A is available in 18 pin dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	5	V
V_i	Input voltage	V_{SS} -0.5 to V_{DD} +0.5	V
P_{tot}	Total power dissipation	400	mW
T_{op}	Operating temperature range	-25 to +50	°C
T_{stg}	Storage temperature range	-65 to +85	°C

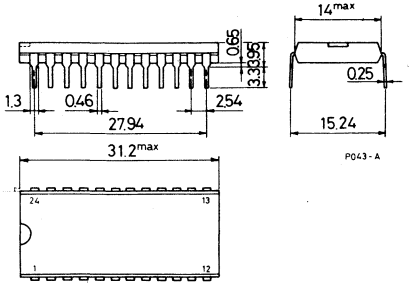
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are referred to V_{SS} pin voltage.

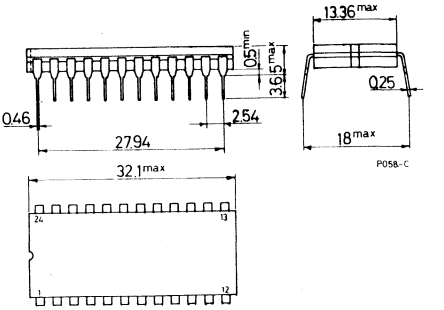
ORDERING NUMBERS:
M760 B1 for dual in-line plastic package
M760A B1 for dual in-line ceramic package (frit seal)
M760 F1 for dual in-line plastic package
M760A F1 for dual in-line ceramic package (frit seal)

MECHANICAL DATA (dimensions in mm)

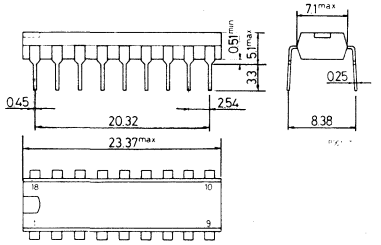
Dual in-line plastic package (M760)



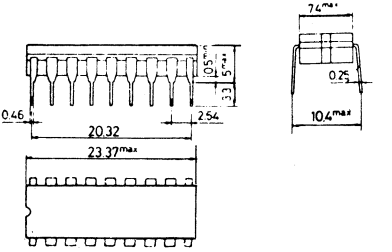
Dual in-line ceramic frit seal package (M760)



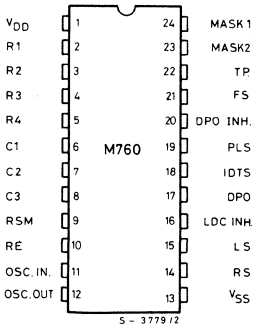
Dual in-line plastic package (M760A)

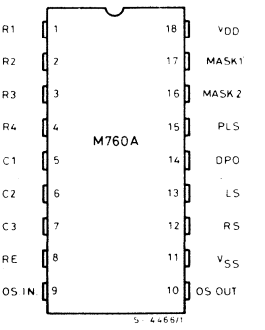


Dual in-line ceramic frit seal package (M760A)

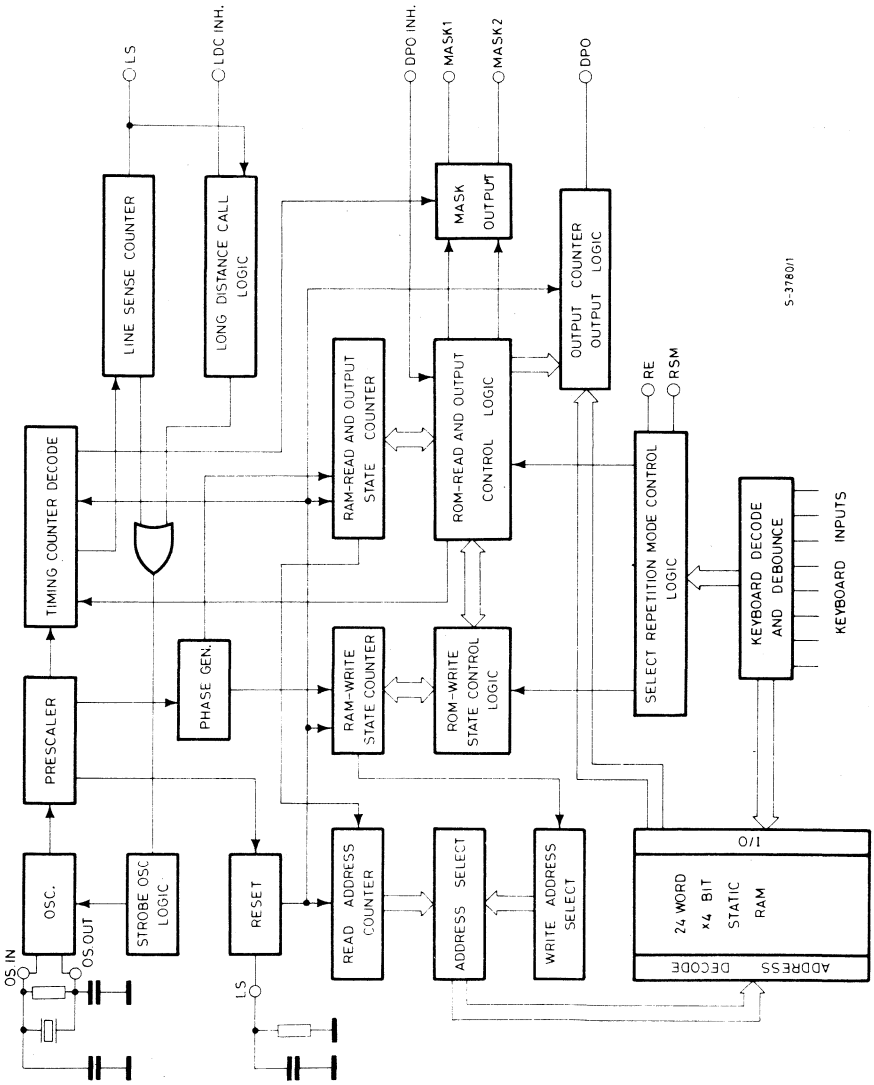


PIN CONNECTIONS





BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (T_{op}= -25°C to +50°C)

	Parameter		Test conditions		Min.	Typ.	Max.	Unit
Supply	V_{DD}	Supply voltage			2.2	2.5	5	V
	I_{DD}	Operating supply current	V_{DD}= 2.5V	f_o= 455 kHz			0.5	mA
	I_{DD} stand-by	Stand-by supply current (oscillator off, no external load connected)	V_{DD}= 2.5V				25	µA
Keyboard inputs	**Row inputs**							
	In_H	Input high current	V_{DD}= 2.5V V_{IH}= 2.5V V_{IL}= 0V			60	80	µA
	In_L	Input low current					-1	µA
	V_{IH}	Input threshold voltage			1			V
	Column inputs							
	I_{IH}	Input high current	V_{DD}= 2.5V V_{IH}= 2.5V V_{IL}= 0V				1	µA
	I_{IL}	Input low current				-60	-80	µA
	V_{IL}	Input threshold voltage					V_{DD}-1V	V
Oscillator	**OSC IN**							
	I_H	Input high current	V_{DD}= 2.5V	V_{IH}= 2.5V			1	µA
	I_L	Input low current	V_{IL}= 0V				-1	µA
	OSC OUT							
	I_{OH}	Output drive current	V_{DD}= 2.5V	V_{OH}= 2V	-150			µA
	I_{OL}	Output sink current	V_{DD}= 2.5V	V_{OL}= 0.5V	150			µA
Mask output	I_{OH}	Output drive current	V_{DD}= 2.2V	V_{OH}= 1.4V	-1			mA
	I_{OL}	Output sink current	V_{DD}= 2.2V	V_{OL}= 0.1V		20		µA
DPO	I_{OL}	Output sink current	V_{DD}= 2.2V	V_{OL}= 0.4V	1			mA
	I_{OFF}	Output leakage current	V_{DD}= 2.5V				+1	µA
LDC INH DPO INH PLS RSM RE	I_{IH}	Input high current	V_{DD}= 2.5V	V_{IH}= 2.5V			1	µA
	I_{IL}	Input low current	V_{DD}= 2.5V	V_{IL}= 0V			-1	µA
	V_{IH}	Input high voltage			0.7V_{DD}			V
	V_{IL}	Input low voltage					0.3V_{DD}	V
LS	I_{IH}	Input high current	V_{DD}= 2.5V	V_{IH}= 2.5V			1	µA
	I_{IL}	Input low current	V_{DD}= 2.5V	V_{IL}= 0V	-100	-160	-250	µA
	V_{IH}	Input high voltage			0.7V_{DD}			V
	V_{IL}	Input low voltage					0.3V_{DD}	V
RS	I_{OH}	Output drive current	V_{DD}= 2.5V	V_{OH}= 1.8V	-20			µA
	I_{OL}	Output leakage current					1	µA
	V_{IH}	Input high voltage			0.8V_{DD}			V
	V_{IL}	Input low voltage					0.2V_{DD}	V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{op} = -25 to +50°C)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_{ACC}	Key access time after last bounce	for all f_o = 455 kHz V_{DD} = 2.5V		5.5		ms
t_{OSC}	Oscillator start-up time				60	ms
t_{MASK}	Mask 1, Mask 2 pulse duration			20		ms
t_{DM}	Mask 1, Mask 2 delay time with respect to DPO			50		ms
t_{PD}	Pre-digital pause			400		ms
t_{DPO}	DPO period FS = 0 FS = 1			50 100		ms ms
t_B/t_M	Break to make ratio			1.6		
t_{IDT}	Interdigit time IDTS = 0 IDTS = 1			800 400		ms ms
t_{RES}	Minimum line break before reset			150		ms
t_{OTO}	Oscillator turn-off time after clear-down. LDC Inh = 0 LDC Inh = 1			 150 300		 ms ms
$t_{LDC\ Inh}$	Line break time when LDC Inh = 1			300		ms

FUNCTIONAL DESCRIPTION

Oscillator (OS IN – OS OUT)

The oscillator has been designed to work with an inexpensive ceramic resonator; (f_o= 455 kHz) it requires two external load capacitors (100 pF) and the inverter feedback resistance.
The oscillator starts after LS (line sens) is taken low; it comes back to the stand-by mode after LS has gone high for at least 150 ms (or 300 ms if LDC-INH high).

Keyboard (R_1 to R_4, C_1 to C_3)

M760 is designed to work with a single contact keyboard.
A valid key entry is recorded when a single row pin is connected to a single column pin.
All the input combinations except a single row and a single column are not recognized.
A valid key is entered after 5 ms from the last key bounce.

Outpulsing inhibition (DPO, INH)

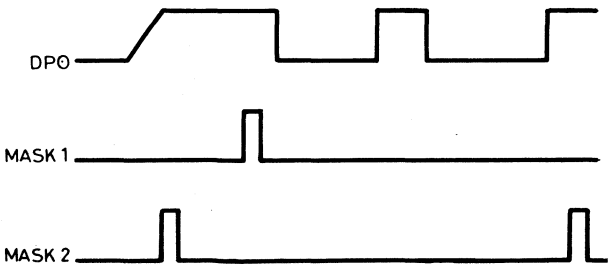
If this pin is low, digits can be entered into the memory but they are not sent on the line; when DPO INH goes high the stored digits are sent on the line.
This function is realized to allow operations with payment-card telephones in which it is sometimes needed to assess the validity of the payment-card.

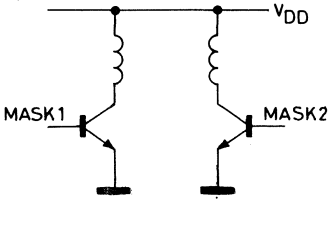
Dial pulse output (DPO)

When a valid key is recognized the line must be opened and closed at a fixed rate and the total number of break pulses corresponds to the number of the selected key (10 line breaks are associated to the key "0").
DPO is an open drain output; line breaks occur when DPO is active to ground.

Mask Outputs (MASK 1, MASK 2)

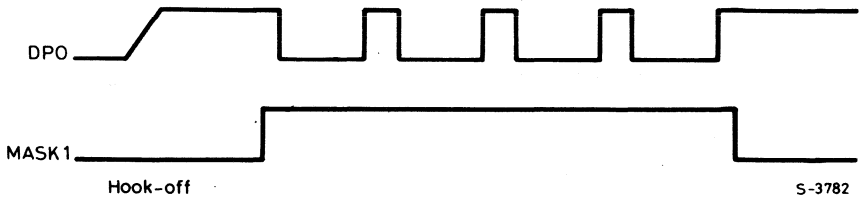
The Mask outputs are used to mute the speech circuit during signalling.
In telephones using conventional speech circuits muting is generally achieved by short-circuiting with a two-winding, bistable reed-relay. In this case MASK 1 and MASK 2 provide pulse outputs to drive the winding which close and open the contact respectively.





FUNCTIONAL DESCRIPTION (continued)

In telephones with electronic speech circuits muting is implemented electronically. In this case a metal option transforms MASK 1 into a signal which remains high throughout signalling.



Redial enable (RE)

Redial of the last call is possible according to the procedures described below only if RE is high.
Redial is never allowed when RE is low.

Redial Selection Mode (RSM)

The last number redialling facility operates in two modes. In the first (RSM high) the key sequence **0 will repeat the last number dialled. The last number memory can be cleared by the # key.
In the second case (RSM low) the last number dialled is only stored if the key * is pressed before replacing the handset. As before, the sequence **0 starts the last number repeat.
In both cases the stored number is unaffected by incoming calls.
The redial request can be simplified by a mask option to the single key *, instead of the sequence **0.

Pause length selection (PLS)

Interdigit pauses are available to interrupt outpulsing to give to the exchange the possibility of switching from a private to a public line.
The device memorizes automatically a pause when the first digit is 0; a maximum of 7 pauses can be added during dialing by selecting key *.
These pauses are active only during redialing and have a duration of 3 sec if PLS is low or 20 sec if PLS is high; in both cases pause duration can be shortened pushing key *.

Line sense (LS)

This input senses if the line loop is closed or not

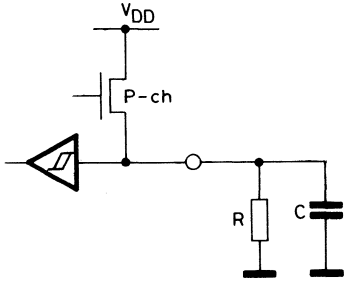
LS = high means loop open
LS = low means loop closed

When LS is kept high for more than 150 ms the circuit is reset (if LDC INH = 0).
When LDC INH = 1 reset occurs after 300 ms.

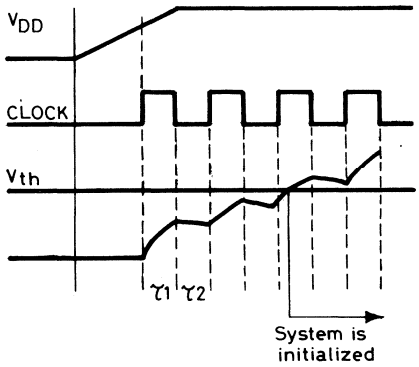
FUNCTIONAL DESCRIPTION (continued)

Reset (RS)

This input/output pin is used to turn off the oscillator when line interrupts of more than 150 ms are sensed; it is also used as a power-on reset in applications where redial is not allowed.
When the hand-set is picked-up and V_{DD} increases over its minimum value, the oscillator starts and an external capacitor is charged above a fixed threshold level by an open drain P-ch. transistor driven by a 150 kHz clock.
Reset occurs after a line interrupt of more than 150 ms; the pull-up transistor goes off and the capacitor discharges through a resistance to GND level.



S-3783



Long distance call inhibit (LDC INH)

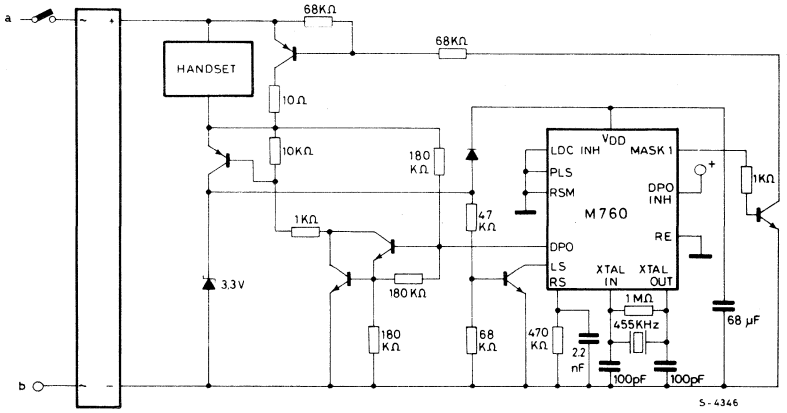
When this input is taken high long distance calls are inhibited; if the first digit is a 0 DPO goes low interrupting the line for a time longer than 300 ms.
The same applied when fraudulent dialing is tried with the hook or any external device by sensing the line condition at the input LS.
When INH is low this facility is inoperative.

Test pin (TP)

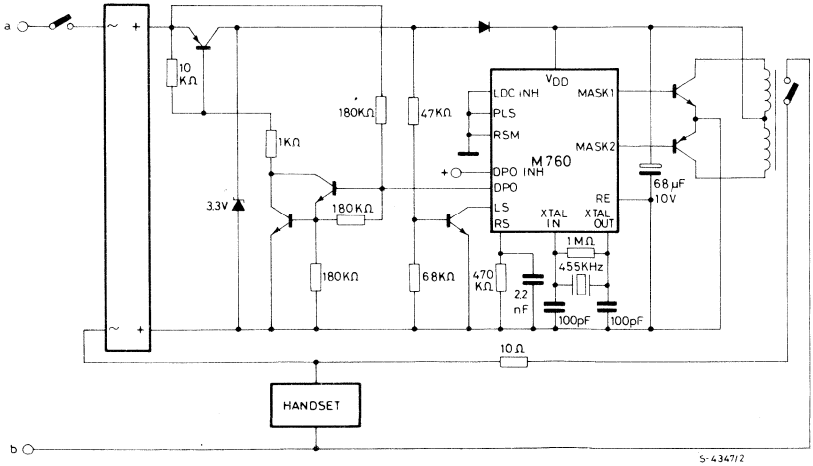
When this input is taken low all the timing values are divided by 100. In this way the length of the testing operations is greatly reduced. This pin has an internal pull-up.

TYPICAL APPLICATIONS

Typical serial applications

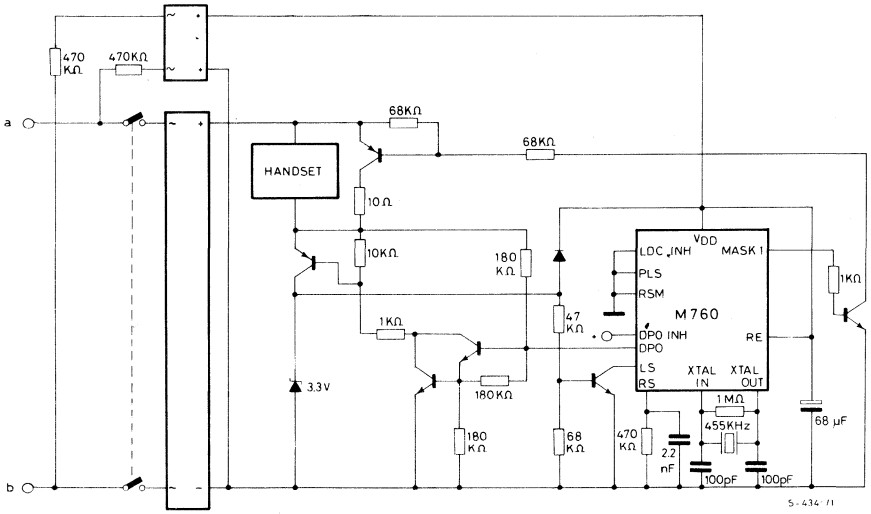


With bistable relee

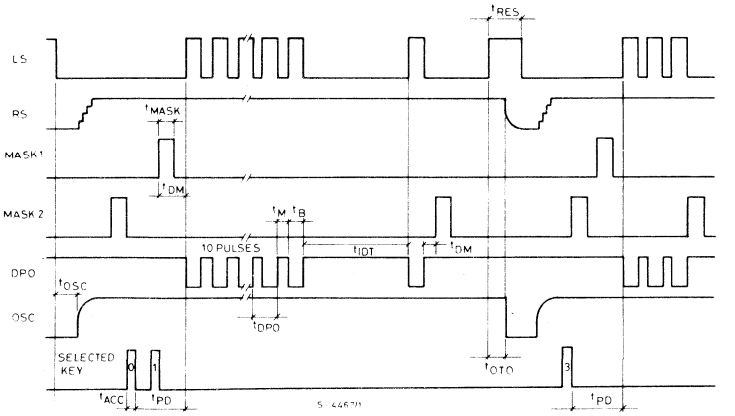


TYPICAL APPLICATIONS (continued)

Pulse dialler with redial



TIMING DIAGRAM



COS/MOS INTEGRATED CIRCUITS

M 761
M 761A

PRELIMINARY DATA

DUAL TONE MULTIFREQUENCY GENERATOR

- 2.5 TO 5V SUPPLY RANGE
- VERY LOW POWER CONSUMPTION
- INTERNAL PULL--UP OR PULL-DOWN RESISTOR WITH DIODE PROTECTION ON ALL KEYBOARD INPUTS
- ON-CHIP CRYSTAL CONTROLLED OSCILLATOR (f_o= 4.433619 MHz) WITH INTEGRATED FEEDBACK RESISTOR AND LOAD CAPACITORS
- LOW HARMONIC DISTORTION
- FIXED PRE-EMPHASIS ON HIGH-GROUP TONES
- FAST START-UP TIME
- LOW POWER CONSUMPTION IN STAND-BY MODE
- MUTE OUTPUT (M761 ONLY)
- ONE CONTACT PER KEY

The M761-M761A provides all the tone frequency pairs required for a DTMF Dialling System. Tones are obtained from an inexpensive TV crystal (f_o= 4.433619 MHz) followed by two independent programmable dividers. The dividing ratio is controlled by the selected key. Keyboard format is 4 rows x 4 columns and a key is valid when a column and a row are connected together.
Internal logic prevents the transmission of illegal tones when more than one key is pressed. Individual tones can be obtained by grounding a column input or connecting a row input to V_{DD}. If no key is selected the oscillator turns off and the linear parts are strobed to decrease the total power consumption. A debounce output is available, for M761 only, to indicate that a key has been selected. D/A conversion is accomplished by a capacitive network allowing very low power consumption, very low distortion and an exceptional stability of tone level against temperature variations.
The tones are mixed in a resistive network; a unity gain amplifier is provided to realize a two pole active filter with only four external passive components.
SGS-ATES has also developed the LS342, DTMF line interface, which provides the stabilized supply for the M761-M761A from the telephone line and amplifies the output tones to the standardized levels. The M761 can also be interfaced with LS156 speech circuit with MF interface avoiding the need of the common spring set.
The M761 utilizes low voltage COS/MOS technology and is available in 18 pin dual in-line plastic or ceramic package; the M761A is available in 16 pin dual in-line package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} **	Supply voltage	-0.5 to +5.5	V
V_I	Input voltage	-0.3 to V_{DD} +0.5	V
P_{tot}	Power dissipation	400	mW
T_{op}	Operating temperature range	-25 to +50	°C
T_{stg}	Storage temperature range	-55 to +125	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are referred to V_{SS} pin voltage.

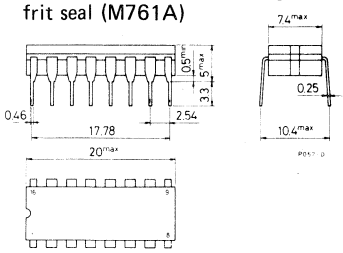
ORDERING NUMBERS: M761 B1, M761A B1 } for dual in-line plastic package

M761 F1, M761A F1 } for dual in-line ceramic package (frit seal)

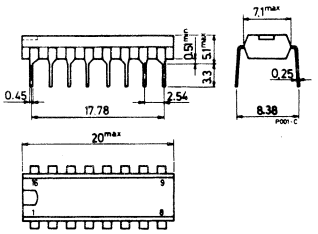
M 761
M 761A

MECHANICAL DATA (dimensions in mm)

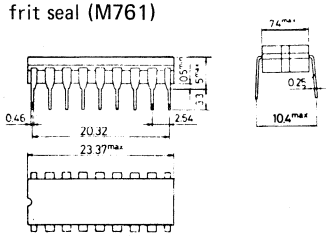
Dual in-line ceramic package frit seal (M761A)



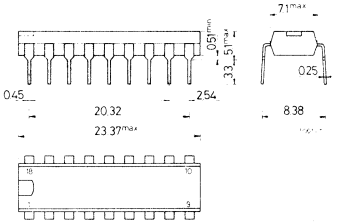
Dual in-line plastic package (M761A)



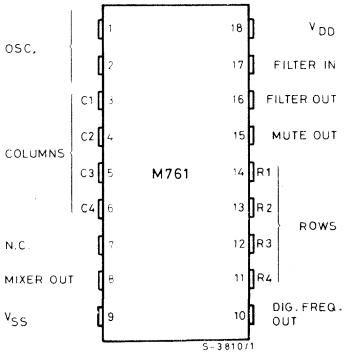
Dual in-line ceramic package frit seal (M761)

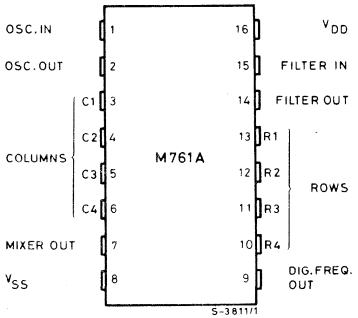


Dual in-line plastic package (M761)

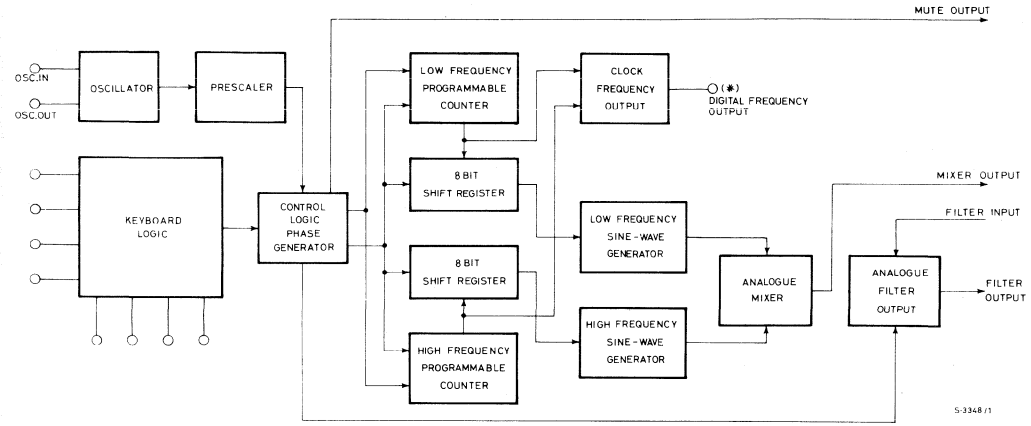


PIN CONNECTIONS





BLOCK DIAGRAM



(*) Not connected in M761A.

ELECTRICAL CHARACTERISTICS (All parameters are tested at T_{amb}= 25°C)

Parameter			Test conditions (see note 1)		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS								
Supply	V_{DD}	Voltage supply voltage			2.5	3	5	V
	I_{DD}	Operating supply current	V_{DD}= 2.5V				2	mA
	I_{DDO}	Stand-by supply current					0.5	mA
Row inputs	I_{IH}	High level input current	V_{DD}= 2.5V	V_{IH}= 2.5V		60	80	µA
	I_{IL}	Low level input current	V_{DD}= 2.5V	V_{IL}= 0V			1	µA
	V_{IH}	High level input threshold voltage			1			V
Column inputs	I_{IH}	High level input current	V_{DD}= 2.5V	V_{IN}= 2.5V			1	µA
	I_{IL}	Low level input current	V_{DD}= 2.5V	V_{IL}= 0V		-60	-80	µA
	V_{IL}	Low level input threshold voltage					V_{DD}-1V	V
Oscillator	I_{IH}	High level input current	V_{DD}= 3V	V_{IN}= 3V			1	µA
	I_{IL}	Low level input current	V_{DD}= 3V	V_{IL}= 0V			1	µA
	I_{OH}	High level output	V_{DD}= 2.5V	V_{OH}= 2V	-300	-500		µA
	I_{OL}	Low level output current	V_{DD}= 2.5V	V_{OL}= 0.5V	300	500		µA
Digit. freq. outp.	I_{OL}	Low level output current (open drain output)	V_{DD}= 3V	V_{OL}= 1V	200			µA
Filter	V_O	Output DC voltage without tones	V_{DD}= 2.5V				200	mV

ELECTRICAL CHARACTERISTICS (continued)

		Parameter	Test conditions (see note 1)	Min.	Typ.	Max.	Unit
Filter	V_O	Output DC voltage with 2 tones	V_{DD}= 2.5V (see note 2)	0.81	0.84	0.87	V
Mute outputs	I_{OH}	Output drive current	V_{DD}= 2.5V V_{OH}= 1.5V	-100			µA
	I_{OL}	Output sink current	V_{DD}= 2.5V V_{OL}= 1V	20			µA

AC CHARACTERISTICS

Oscillator	R_F	Feedback oscillator resistance		4	4.5		MΩ
	C_I	Input capacitance to V_{DD}			9.5	10.5	pF
	C_O	Output capacitance to V_{DD}			10.5	11.5	pF
Mixer	Z_{O1}	Output dynamic impedance with 2 tones	V_{DD}= 2.5V		10		kΩ
Filter	Z_{O2}	Output dynamic impedance with 2 tones	V_{DD}= 2.5V		2.5		kΩ
Tone characteristics	$\frac{\Delta F}{F}$	Max. output tone deviation from standard R_1 697 Hz R_2 770 Hz R_3 852 Hz R_4 941 Hz C_1 1209 Hz C_2 1336 Hz C_3 1477 Hz C_4 1633 Hz	At crystal frequency f = 4.433619 MHz			 +0.5 -0.2 +0.5 -0.6 +0.6 -0.4 -0.3 +1.1	 % % % % % % % %
	V_{LF}	Low frequency tones amplitude at filter out	V_{DD}= 2.5V (see note 3)	150	175	200	mVpp
	V_{HF}	High frequency tones amplitude at filter out	V_{DD}= 2.5V (see note 3)	195	220	245	mVpp
		Pre-emphasis		1	2	3	dB
		Unwanted frequency components at f = 3.4 kHz at f = 50 kHz				 -33 -80	 dBm dBm
		Total harmonic distortion for a single frequency	V_{DD}= 2.5V			2	%
	t_s	Start up time	V_{DD}= 2.5V (see fig. 1) (see fig. 2)		3	5	ms
	t_r	Supply voltage rise time	V_{DD}= 2.5V			250	ms

Note 1: This device has been designed to be connected to LS342 MF tone dialler line interface, from which it takes a V_{DD}= 2.5V min. therefore many parameters are tested at this value.

Note 2: The value of DC output component at two different conditions of supply voltages, with two tones activated, can be related as follows:

$$V_{DC'} = V_{DC} \frac{V_{DD'}}{V_{DD}}$$

Note 3: The value of AC output components (V_{LF}, V_{HF}) at two different conditions of supply voltages can be related as follows:

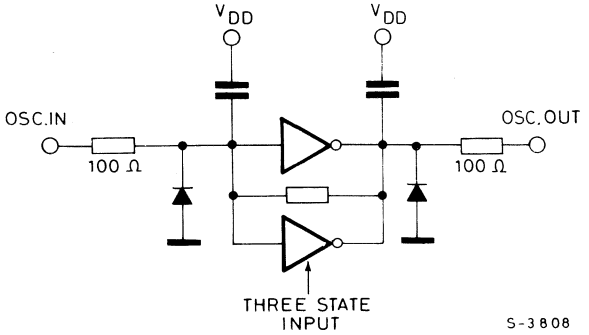
$$V_{LF'} = V_{LF} \frac{V_{DD'}}{V_{DD}} \qquad V_{HF'} = V_{HF} \frac{V_{DD'}}{V_{DD}}$$

The values are measured with one tone at the output.

FUNCTIONAL DESCRIPTION

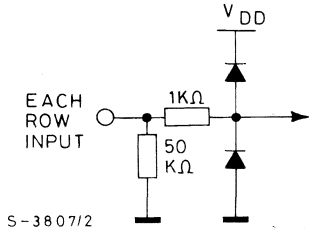
Oscillator (OSC. IN – OSC. OUT)

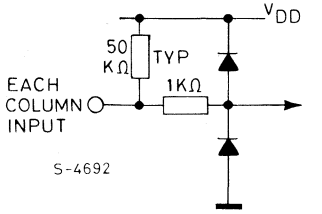
The oscillator circuit has been designed to work with a 4.433619 MHz crystal ensuring both fast start-up time and low current consumption.
When V_{DD} is applied and a key is activated two inverters are paralleled (see fig. below) to decrease the total r_{on} resistance.
After oscillations have started one of the two buffers is switched off and the current consumption is reduced to 2/3 of the initial value.
Feedback resistance and load capacitances are integrated on the chip ensuring good temperature performance.
When the device is supplied but no key is activated, the oscillator is in the stand-by mode to minimize power consumption.



Keyboard inputs ($C_1, C_2, C_3, C_4 - R_1, R_2, R_3, R_4$)

Each keyboard input has an internal protection circuit; columns have pull-up resistances while rows have pull-down resistances.
If a column input is grounded the corresponding single tone is generated; the same applies when a row input is connected to V_{DD}. When a single column input is connected to a single row input a dual tone is generated.
When two or more column or row inputs are activated no tone is generated.

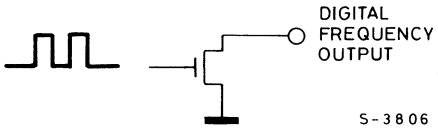




FUNCTIONAL DESCRIPTION (continued)

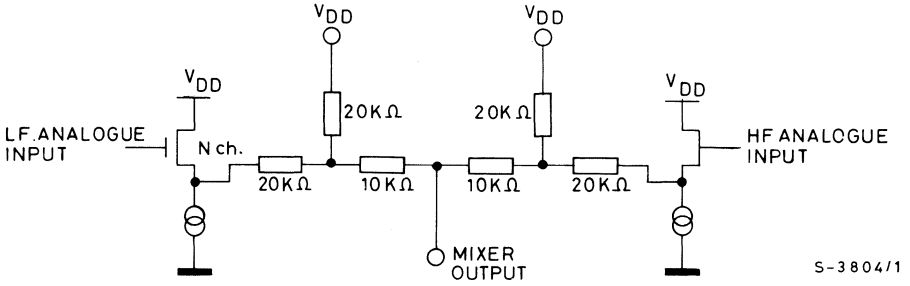
Digital frequency output

This output is intended for testing only; when a single tone is activated, at this output is available digital signal whose frequency is 16 times the selected output tone frequency. This output is an oper collector N-channel transistor.



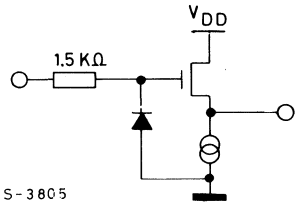
Mixer output

The two reconstructed sine waves are buffered then mixed in a resistive array network that also restores the DC output level.



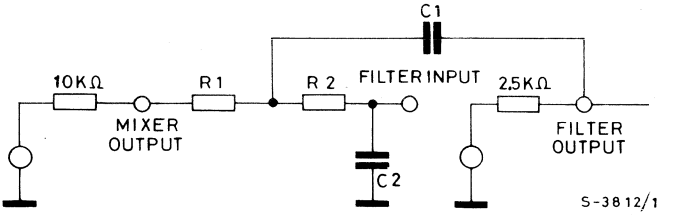
Filter (Filter input, filter output)

A unity gain amplifier is available to realize a two pole active filter (see fig. below). The output of this amplifier is held low until tones are valid, it than rises to about 0.85V at V_{DD}= 2.5V. Tones are superimposed on this DC.
The output DC component is very precise and stable to allow DC coupling with the LS342 DTMF line inteface and LS156 speech circuit with MF interface.



FUNCTIONAL DESCRIPTION (continued)

The output dynamic impedance of the filter is about 2.5 kΩ.
The following equivalent circuit should be applied during filter design:



It is evident that R_1 and R_2 should be kept high to avoid undue influence of Mixer and Filter output impedances.
The following values are suggested:

R_1= 430 kΩ ± 2% – R_2= 82 kΩ ± 2% – C_1= 820 pF ±10% – C_2= 120 pF ±10%

Mute output

Mute output becomes active when a key is activated eliminating keyboard bounces and remains active for all the duration of tone transmission.
If the key is released before the oscillator produces the correct control signals, mute output is disabled.

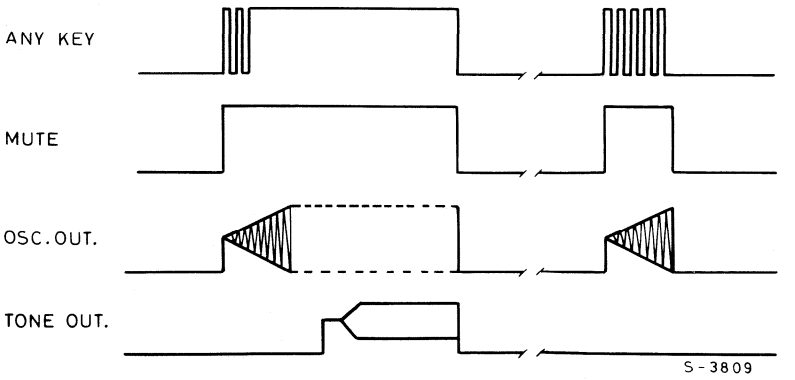


Fig. 1 - Start-up time measurement test set

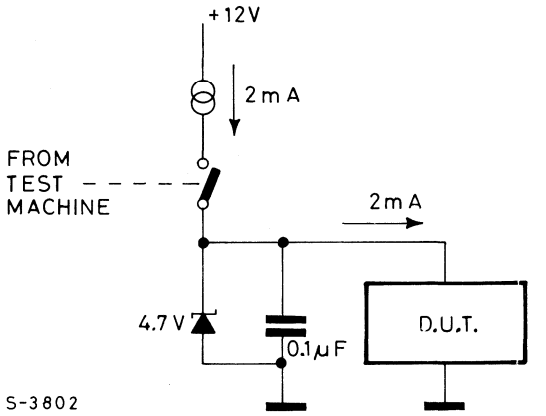
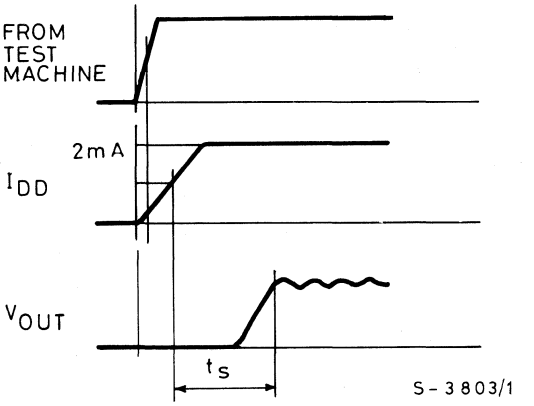
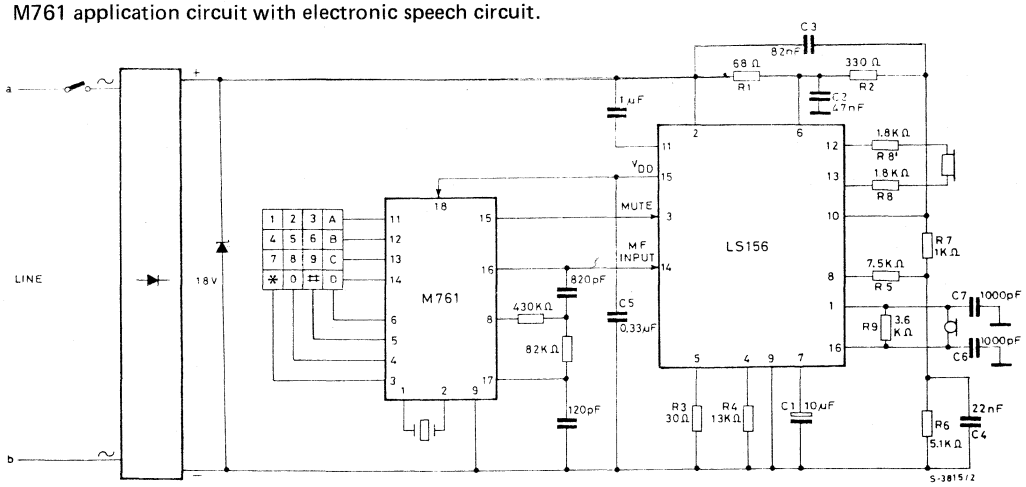


Fig. 2 - Start-up time definition

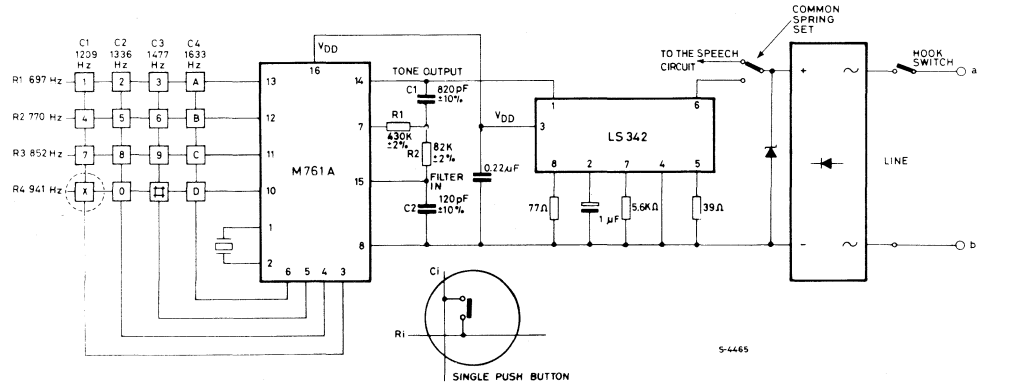


TYPICAL APPLICATIONS

M761 application circuit with electronic speech circuit.



M761A application circuit with LS342 line interface



COS/MOS INTEGRATED CIRCUITS

M 764
M 764A

ADVANCE DATA

TONE RINGER

- WIDE OUTPUT TONE SELECTION
- DIRECT DRIVE FOR PIEZOCERAMIC OR DYNAMIC TRANSDUCERS
- BUILT IN BAND PASS FILTER (20 TO 60Hz)
- μP CONTROL INPUT

The M764 is a high performance electronic ringer suitable for application in standard and parallel connection telephones; it can also be used as an alarm indicator. An incorporated bandpass filter prevents spurious ringing caused by transients and dialling pulses. Pin-selectable options permit three, two and single tone sequences.
The output stage allows direct drive of both piezoceramic and dynamic transducers. The output tone level can be externally programmed to increase gradually during the first three bursts. Output tone stability and the bandpass filter corner frequencies are guaranteed by a crystal controlled oscillator. The M764 utilizes COS/MOS technology and is available in 18 pin dual in-line plastic or ceramic package; the M764A is available in 16 pin dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS *

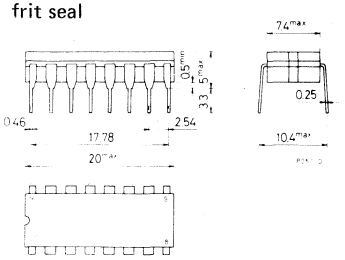
V_{DD}	Supply voltage	-0.5 to +20	V
V_I	Input voltage	-0.3 to V_{DD} + 0.5	V
P_{tot}	Power dissipation	400	mW
T_{op}	Operating temperature range	-25 to 80	°C
T_{stg}	Storage temperature range	-55 to 125	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

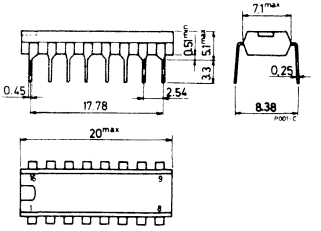
ORDERING NUMBERS:
M 764 B1 for dual in-line plastic package
M 764A B1 for dual in-line plastic package
M 764 F1 for dual in-line frit seal ceramic package
M 764A F1 for dual in-line frit seal ceramic package

MECHANICAL DATA (Dimensions in mm)

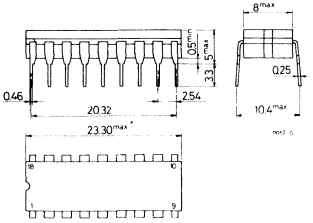
Dual in-line ceramic package (M764A)
frit seal



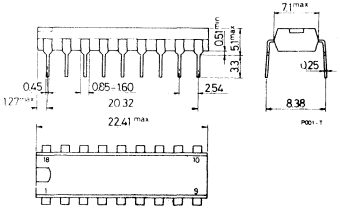
Dual in-line plastic package (M764A)



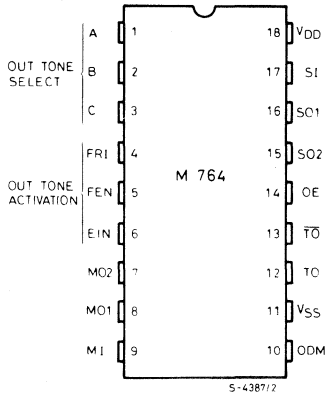
Dual in-line ceramic package (M764)
frit seal

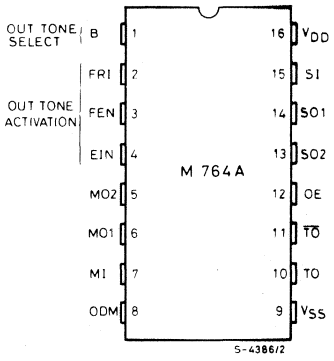


Dual in-line plastic package (M764)

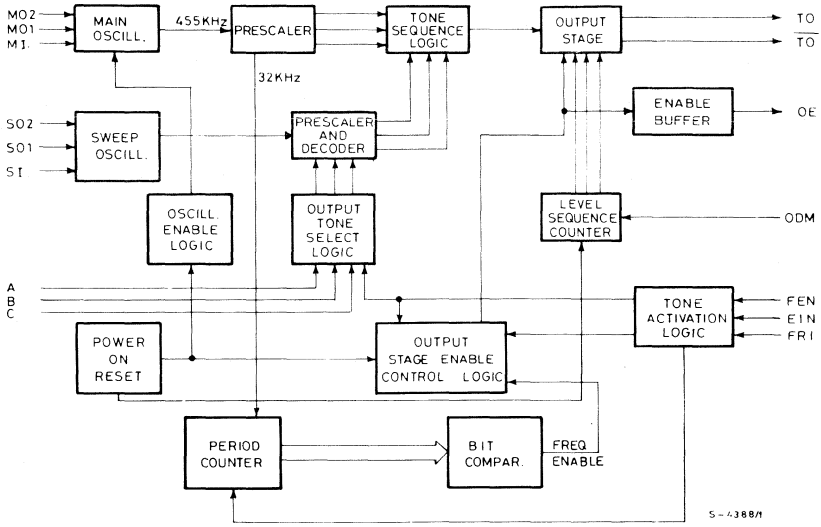


PIN CONNECTIONS





BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (All parameters are tested at $T_{amb} = 25°C$)

Parameter			Test conditions		Min.	Typ.	Max.	Unit
DC CHARACTERISTICS								
Supply	V_{DD}	Voltage supply			6		18	V
	V_{TH}	Power on/off reset threshold			4.5		5.5	V
	V_{TH}	Sequence logic power on/off reset			1.8		2.8	V
	I_{DD}	Operating supply current	V_{DD}= 15V OE = 1				0.5	mA
	I_{DDO}	Stand-by supply current	V_{DD}= 15V				0.15	mA
Main oscillator	M_I	Main oscillator input	I_{IH} V_{IH}= 15V	V_{DD}= 15V			+5	µA
			I_{IL} V_{IL}= 0V				-1	
	M_{O1}	Main oscillator output 1	I_{OH} V_{OH}= 14V	V_{DD}= 15V			-250	µA
			I_{OL} V_{OL}= 1V				+250	
	M_{O2}	Main oscillator output 2	I_{OH} V_{OH}= 14V	V_{DD}= 15V			-200	µA
			I_{OL} V_{OL}= 1V				+200	

ELECTRICAL CHARACTERISTICS (continued)

	Parameter		Test conditions		Min.	Typ.	Max.	Unit
Sweep oscillator	S_I	Sweep oscillator input	I_{IH} V_{IH}= 15V	V_{DD}=15V			+1	µA
			I_{IL} V_{IL}= 0V				-1	
	S_{O1}	Sweep oscillator output 1	I_{OH} V_{OH}= V_{DD}-1V	V_{DD}=15V		-200		µA
			I_{OL} V_{OL}= V_{DD}-3V			+200		
	S_{O2}	Sweep oscillator output 2	I_{OH} V_{OH}= V_{DD}-1V	V_{DD}=15V		-200		µA
			I_{OL} V_{OL}= V_{DD}-3V			+200		
Control pins	EIN FEN ODM	Enable input Filter enable input Output drive mode			Standard C/MOS inputs			
	A B C	Output sequence selection pins			C/MOS inputs with active pull-down			
Freq. input	FRI	Frequency input	I_{IL} V_{IL}= 0V				1	µA
			I_{IH} V_{IH}= 4V		8		16	
			V_{TH}		2		4	V
Output enable	OE		I_{OH} V_{DD}= 15V V_O = 13V		10			mA
			I_{OL} V_{DD}= 15V V_O = 1V		1			
Tone outputs	TO	Output	I_{OH} V_{DD}= 15V V_O = 14V		10			mA
			I_{OL} V_{DD}= 15V V_O = 0.7V		10			
	$\overline{TO}$	Inverted output	I_{OH} V_{DD}= 15V V_O = 14V		10			mA
			I_{OL} V_{DD}= 15V V_O = 0.7V		10			

AC CHARACTERISTICS

Main oscillator	t_{SM}	Start up time	V_{DD}= 6V f_o= 455 KHz			10		ms
			R_F= 1 MΩ C_I= C_O= 100 pF	see tables 1-2				
Sweep oscill.	t_{SS}	Start up time	V_{DD}= 6V f = 1140 to 11400 Hz (*)			5		ms

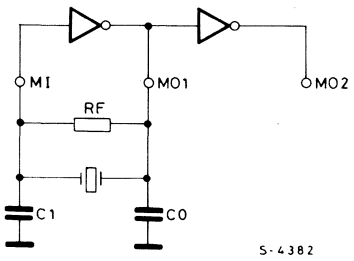
(*) R > 50 KΩ
C > 100 pF

FUNCTIONAL DESCRIPTION

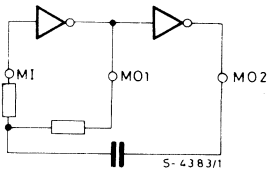
Main oscillator

The main oscillator has been designed to be driven either by an external RC network or by a ceramic resonator (see fig. 1):

Fig. 1 - a) Crystal controlled oscillator



b) RC oscillator



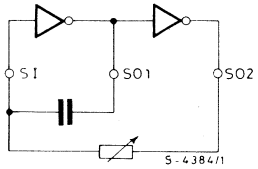
The accuracy of the output tones and of the band-pass filter characteristics are determined by the accuracy of the main oscillator frequency.
The crystal guarantees good performance over the whole temperature range with no external trimmer.
The main oscillator as well as the sweep oscillator are maintained in a stand-by condition or forced to run according to table 1.

Sweep oscillator

The sweep oscillator (fig. 2) controls the repetition rate of the output tone sequence. The output repetition period is given by

$$T_{rep} = \frac{384}{F_{sweep\ oscill.}}$$

Fig. 2

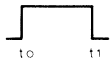
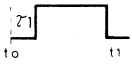
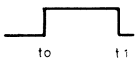
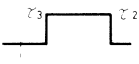
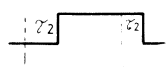
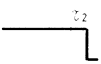
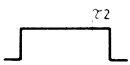
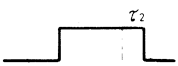


Output tone activation (pins FEN, EIN, FRI)

The output stage is enabled by the signal OE (output enable) under control of pins FEN, EIN, FRI as shown in table 1, and fig. 3.
Pin FEN and EIN are standard C-MOS inputs.
Pin FRI has a pull-down resistor of approximately 300 KΩ.

FUNCTIONAL DESCRIPTION (continued)

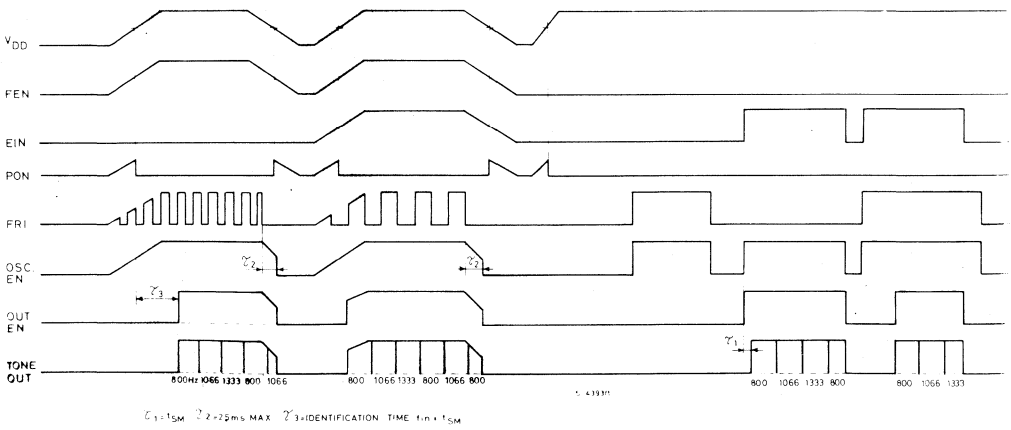
Table 1

FEN	EIN	FRI	OSC. EN.	OUT. EN.	TONE OUT
0	0	0	0	0	0
0	0	1	1	0	0
0		0			
0		1	1		
1	0			 IF fmin < f < fmax	
1	1			 IF f > fmin	

S-4392/1

$\tau_1 = t_{SM}$ $\tau_2 = 25ms$ MAX τ_3 = IDENTIFICATION TIME $f_{in} + t_{SM}$

Fig. 3 – Timing diagram



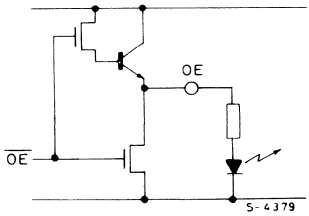
$\tau_1 = t_{SM}$ $\tau_2 = 25ms$ MAX τ_3 = IDENTIFICATION TIME $f_{in} + t_{SM}$

FUNCTIONAL DESCRIPTION (Continued)

Output enable (OE)

The output enable pin (OE) can be used in special application to drive a LED or any external circuit to indicate that an incoming ringing signal has been detected by the tone ringer as in automatic responders. OE timing diagrams are shown in table 1.
The OE output stage configuration is shown in fig. 4.

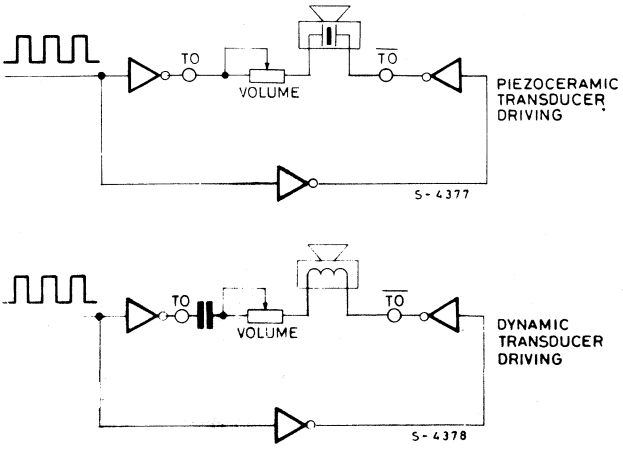
Fig. 4



Tone outputs (TO, $\overline{TO}$)

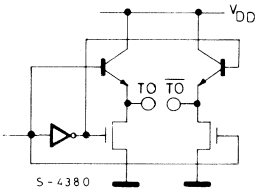
Two complementary outputs are provided to drive in a bridge configuration both piezoceramic and dynamic transducers (see fig. 5).

Fig. 5



The configuration of the output buffer is shown in fig. 6.

Fig. 6



The output waveform is a square wave with 50% duty cycle.
The generated tone level can be constant or can be gradually increased up to the max. level during the detection of the first three ring signal.
This function has been implemented controlling the output voltage swing that can be V_{DD} for max. output level, 0.4 V_{DD} for the intermediate output level and 0.1 V_{DD} for the lowest output level.

Output drive mode (ODM)

The output level is constant if this pin is a logical 0: it gradually increases to the max. level if this pin is a logical 1: the sequence can take place if after the first ring signal during the ring tone pause period the supply does not fail below the power on reset threshold (2.8V) and starts always from the lowest level.

Output tone selection (A B C)

Table 2

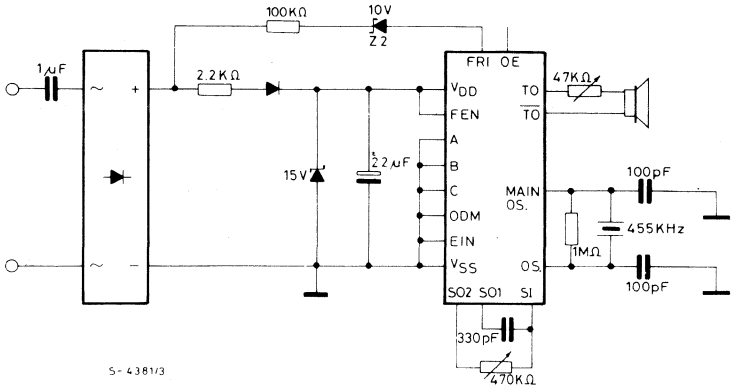
A	B	Output tone sequences and frequencies $f_{main\ oscill.}$ = 455 KHz and pin C = 0		
0	0	800	1066	1333
0	1	800	1066	
1	1	800	d.c. 50%	
1	0	800		

All the above mentioned frequencies are divided by 2 when pin C is taken to V_{DD}.

In the M764A pins A and C are not available and are internally pulled down.

TYPICAL APPLICATIONS

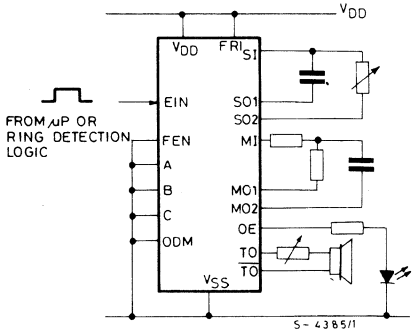
a) **Tone ringer for standard telephone applications**



If pin EIN is connected to V_{DD} the ringer is activated by frequencies upper than 20Hz.

- In both cases the volume potentiometer can be avoided connecting the ODM to V_{DD} allowing the gradually increase of the ringer volume in three steps.
- The number of the output available tones and their frequencies are controlled by ABC pins according to table 2.

b) **Tone ringer for alarm, buzzer or ring tone detection in centralized equipments.**



The number of the output available tones and their frequencies are controlled by ABC pins according to table 2.

COS/MOS INTEGRATED CIRCUIT

M 1024

NOT FOR NEW DESIGN

30-CHANNEL REMOTE CONTROL TRANSMITTER

- LOW POWER DISSIPATION IN TRANSMISSION
- QUASI-ZERO STAND-BY CURRENT
- WIDE SUPPLY VOLTAGE RANGE
- INPUTS FULLY PROTECTED
- HIGH NOISE IMMUNITY
- INTERLOCK PREVENTS INCORRECT SELECTION

The M 1024 is a monolithic integrated circuit intended for remote controlled systems in which 30 different ultrasonic frequencies are used to transmit 30 commands.
The M 1024 comprises an oscillator circuit, a variable and a fixed frequency divider, a decoder and a command error protection. The circuit is produced in COS/MOS technology. In conjunction with the ultrasonic Receiver M 1025 a complete remote control system can be realized. The device is available in a 16-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	0.5 to 12	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
$\|I_O\|$	Output current	10	mA
P_{tot}	Total power dissipation	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	-25 to 70	°C

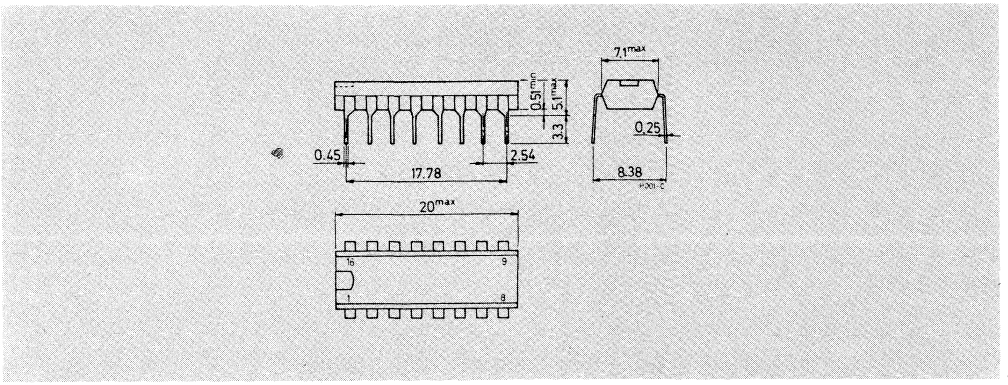
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages value are referred to V_{SS} pin voltage.

ORDERING NUMBER: M 1024 B5

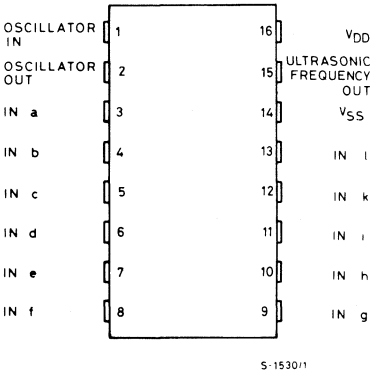
MECHANICAL DATA

Dimensions in mm

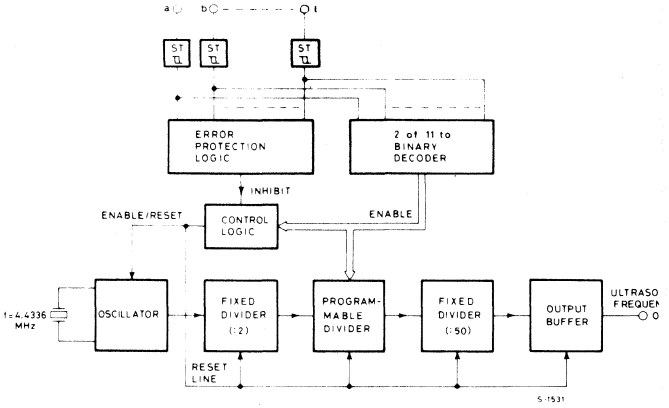


M 1024

PIN CONNECTIONS



BLOCK DIAGRAM



TRUTH TABLE (f_i = 4.4336 MHz)

Channel Number	Inputs											Output Frequency
	a	b	c	d	e	f	g	h	i	k	l	
1	H	H	H	H	L	H	H	L	H	H	H	33 945 Hz
2	H	H	H	H	L	H	H	H	H	H	L	34 291 Hz
3	H	H	H	H	L	H	L	H	H	H	H	34 638 Hz
4	H	H	H	H	L	H	H	H	H	L	H	34 984 Hz
5	H	H	H	H	L	L	H	H	H	H	H	35 330 Hz
6	H	H	H	H	L	H	H	H	L	H	H	35 677 Hz
7	L	H	H	H	H	L	H	H	H	H	H	36 023 Hz
8	L	H	H	H	H	H	H	H	L	H	H	36 370 Hz
9	H	L	H	H	H	L	H	H	H	H	H	36 716 Hz
10	H	L	H	H	H	H	H	H	L	H	H	37 062 Hz
11	H	H	L	H	H	L	H	H	H	H	H	37 409 Hz
12	H	H	L	H	H	H	H	H	L	H	H	37 755 Hz
13	H	H	H	L	H	L	H	H	H	H	H	38 101 Hz
14	H	H	H	L	H	H	H	H	L	H	H	38 448 Hz
15	L	H	H	H	H	H	L	H	H	H	H	38 794 Hz
16	L	H	H	H	H	H	H	H	H	L	H	39 141 Hz
17	H	L	H	H	H	H	L	H	H	H	H	39 487 Hz
18	H	L	H	H	H	H	H	H	H	L	H	39 833 Hz
19	H	H	L	H	H	H	L	H	H	H	H	40 180 Hz
20	H	H	L	H	H	H	H	H	H	L	H	40 526 Hz
21	H	H	H	L	H	H	L	H	H	H	H	40 872 Hz
22	H	H	H	L	H	H	H	H	H	L	H	41 219 Hz
23	L	H	H	H	H	H	H	L	H	H	H	41 565 Hz
24	L	H	H	H	H	H	H	H	H	H	L	41 912 Hz
25	H	L	H	H	H	H	H	L	H	H	H	42 258 Hz
26	H	L	H	H	H	H	H	H	H	H	L	42 604 Hz
27	H	H	L	H	H	H	H	L	H	H	H	42 951 Hz
28	H	H	L	H	H	H	H	H	H	H	L	43 297 Hz
29	H	H	H	L	H	H	H	L	H	H	H	43 643 Hz
30	H	H	H	L	H	H	H	H	H	H	L	43 990 Hz

DESCRIPTION

The truth table shows the 30 ultrasonic transmission frequencies used in the wireless transmission of remote control commands to the receiver. These frequencies are derived from the frequency of a quartz controlled oscillator with the aid of a variable frequency divider operating on the blaking principle. This is accomplished by blanking out between 1 and 30 out of every 128 pulses of the oscillator frequency (4.4336 MHz). The variable divider is preceded by a flip flop which halves the quartz frequency. The variable divider is followed by a fixed divider which divides by 50. It reduces the jitter, which is unavoidable when using the blanking principle, to negligible values. The expression for the ultrasonic output frequency is

$$f_o = \frac{f_i\,(97 + N)}{12\,800}$$

wherein N is the channel number and f_i = 4.4336 MHz (sub-carrier frequency). The space between two adiacent ultrasonic frequencies is 346.4 Hz.

The inputs accept a 2 of 11 code: by connecting simultaneously to V_{SS} one of a to e and one of f to l input, a 5 bit word is generated internally and applied to the variable divider. The relative frequency is thus available at the output.

An error protection circuit prevents incorrect operation. Under these conditions the oscillator will not start to operate, and the frequency divider is held in a defined position.

Since consumption under standby conditions is very low, the ultrasonic transmitter need never be switched off. The selected frequency appears at the output when the threshold voltage is exceeded at the two control inputs. A threshold voltage hysteresis ensures that AC voltages which may be superimposed on the input voltage cannot falsify the actuation.

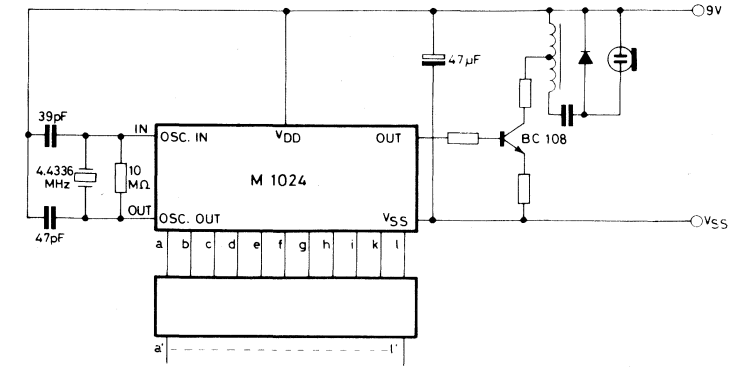
RECOMMENDED OPERATING CONDITIONS

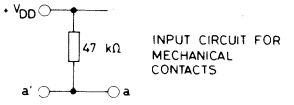
V_{DD}	Supply voltage	7 to 9	V
V_I	Input voltage	0 to V_{DD}	V
f_i	Oscillator frequency	4.4336	MHz
T_{op}	Operating temperature	-25 to 70	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

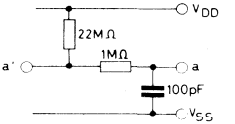
Parameter		Test conditions	Values at 25°C			Unit
			Min.	Typ.	Max.	
I_{CCL}	Quiescent supply current	V_{DD} = 9V all inputs at V_{DD}		2	10	µA
I_{CC}	Supply current	V_{DD} = 9V - oscillator running - ultrasonic freq. output open		1.5	3	mA
I_I	Input current	V_{DD} = 9V V_I = 0 ÷ V_{DD}		|0.01|	|1|	µA
r_{on}	High level output resistance (on state)	V_{DD} = 7V I_{OH} = -1 mA		0.5	1	kΩ
r_{on}	Low level output resistance (on state)	V_{DD} = 7N I_{OL} = 0.2 mA		1.5	3	kΩ
V_{TLH}	Positive going threshold voltage at the inputs a to l	V_{DD} = 9V		4.5		V
V_{THL}	Negative going threshold voltage at the inputs a to l	V_{DD} = 9V		4.1		V

TYPICAL APPLICATION





INPUT CIRCUIT FOR MECHANICAL CONTACTS



INPUT CIRCUIT FOR TOUCH CONTACTS

S-2x001

COS/MOS INTEGRATED CIRCUIT

M 1124

30-CHANNEL REMOTE CONTROL TRANSMITTER

- FEW EXTERNAL COMPONENTS
- INTERLOCK PREVENTS INCORRECT SELECTION
- QUASI-ZERO STAND-BY CURRENT
- WIDE SUPPLY VOLTAGE RANGE
- INPUTS FULLY PROTECTED

The M 1124 is a monolithic integrated circuit intended for remote controlled systems in which 30 different ultrasonic frequencies are used to transmit 30 commands.
The M 1124 comprises on oscillator circuit which does not require external components except the quartz. Further it comprises a fixed and a variable frequency divider, a decoder and a command error protection. All the command inputs are pulled-up to V_{DD} by integrated resistors, to reduce the number of external components. Due to the relative low input impedances, the M 1124 is not suited for touch contacts. The circuit is produced in COS/MOS technology. In conjunction with the ultrasonic receivers M 1025 or M 1130, a complete remote control system can be realized. The device is available in a 16-lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}**	Supply voltage	-0.5 to	12	V
V_I	Input voltage	-0.5 to V_{DD}	+0.5	V
$\|I_O\|$	Output current		10	mA
P_{tot}	Total power dissipation		200	mW
T_{stg}	Storage temperature	-65 to	150	°C
T_{op}	Operating temperature	0 to	70	°C

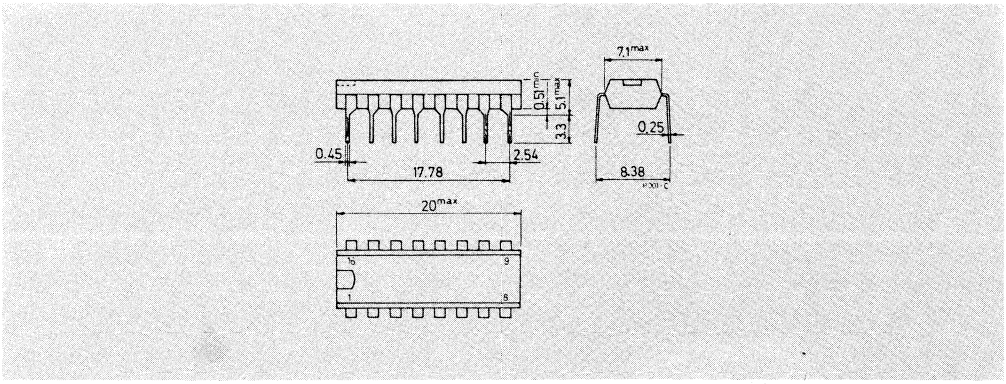
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages are with respect to V_{SS} (GND).

ORDERING NUMBER: M 1024 B1

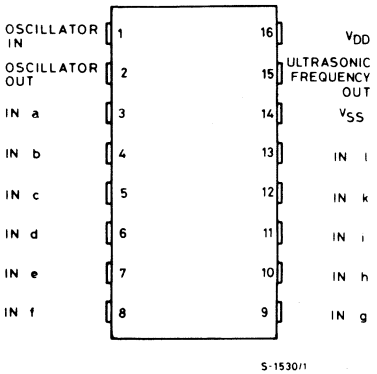
MECHANICAL DATA

Dimensions in mm

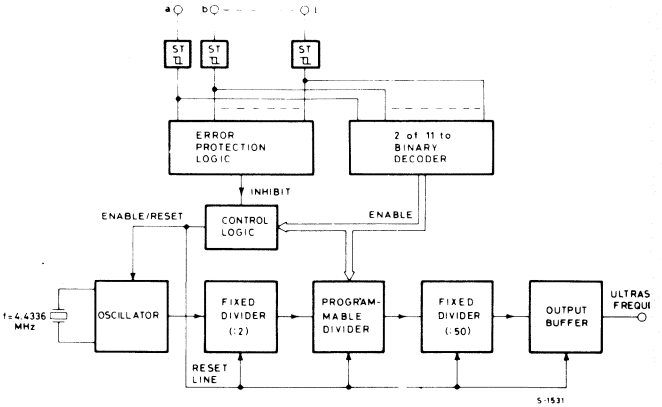


M 1124

PIN CONNECTIONS



BLOCK DIAGRAM



TRUTH TABLE (f_i = 4.4336 MHz)

Channel Number	Inputs											Output Frequency
	a	b	c	d	e	f	g	h	i	k	l	
1	H	H	H	H	L	H	H	L	H	H	H	33 945 Hz
2	H	H	H	H	L	H	H	H	H	H	L	34 291 Hz
3	H	H	H	H	L	H	L	H	H	H	H	34 638 Hz
4	H	H	H	H	L	H	H	H	H	L	H	34 984 Hz
5	H	H	H	H	L	L	H	H	H	H	H	35 330 Hz
6	H	H	H	H	L	H	H	H	L	H	H	35 677 Hz
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8	L	H	H	H	H	H	H	H	L	H	H	36 370 Hz
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12	H	H	L	H	H	H	H	H	L	H	H	37 755 Hz
13	H	H	H	L	H	L	H	H	H	H	H	38 101 Hz
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15	L	H	H	H	H	H	L	H	H	H	H	38 794 Hz
16	L	H	H	H	H	H	H	H	H	L	H	39 141 Hz
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23	L	H	H	H	H	H	H	L	H	H	H	41 565 Hz
24	L	H	H	H	H	H	H	H	H	H	L	41 912 Hz
25	H	L	H	H	H	H	H	L	H	H	H	42 258 Hz
26	H	L	H	H	H	H	H	H	H	H	L	42 604 Hz
27	H	H	L	H	H	H	H	L	H	H	H	42 951 Hz
28	H	H	L	H	H	H	H	H	H	H	L	43 297 Hz
29	H	H	H	L	H	H	H	L	H	H	H	43 643 Hz
30	H	H	H	L	H	H	H	H	H	H	L	43 990 Hz

DESCRIPTION

The truth table shows the 30 ultrasonic transmission frequencies used in the wireless transmission of remote control commands to the receiver. These frequencies are derived from the frequency of a quartz controlled oscillator with the aid of a variable frequency divider operating on the blanking principle. This is accomplished by blanking out between 1 to 30 out of every 128 pulses of the oscillator frequency (4.4336 MHz) divided by 2.

The variable divider is followed by a fixed divider which divides by 50. It reduces the jitter, which is unavoidable when using the blanking principle, to negligible values. The expression for the ultrasonic output frequency is

$$f_o = \frac{f_i\,(97 + N)}{12\,800}$$

wherein N is the channel number and f_i = 4.4336 MHz (sub-carrier frequency). The space between two adiacent ultrasonic frequencies is 346.4 Hz.

The inputs accept a 2 of 11 code: by connecting simultaneously to V_{SS} one of a to e and one of f to l input, a 5 bit word is generated internally and applied to the variable divider. The relative frequency is thus available at the output.

An error protection circuit prevents incorrect operation. Under these conditions the oscillator will not start to operate, and the frequency divider is held in a defined position.

Since consumption under standby conditions is very low, the ultrasonic transmitter need never be switched off. The selected frequency appears at the output when the threshold voltage is exceeded at the two control inputs.

RECOMMENDED OPERATING CONDITIONS

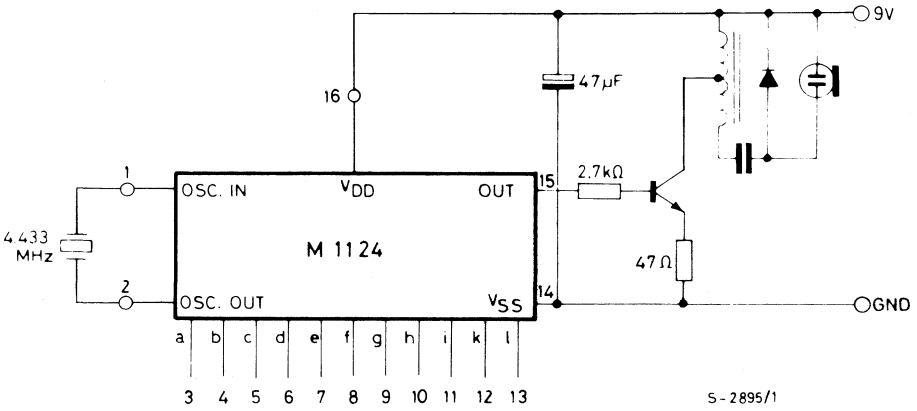
V_{DD}	Supply voltage	6 to 9	V
V_I	Input voltage	0 to V_{DD}	V
f_P	Parallel resonance frequency of the quartz at C_L = 10 pF	4.433	MHz
r_S	Series resistance of the quartz at CL= 10 pF	< 200	Ω
T_{op}	Operating temperature	0 to 70	°C

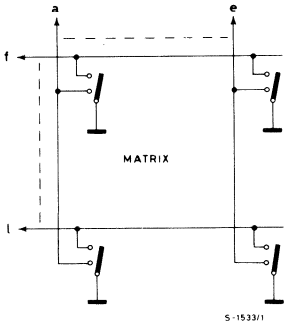
STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

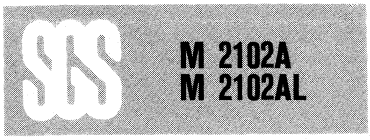
Typical values are at T_{amb}= 25°C, unless otherwise specified.

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{DDL}	Quiescent supply current	All inputs at V_{DD}		2	10	μA
I_{DD}	Supply current	V_{DD} = 9 V - oscillator running - ultrasonic freq. output open		1.5	3	mA
I_I	Input current	V_I= 0		-20		μA
r_{on}	High level output resistance (on state)	I_{OH}= -1 mA		0.5	1	kΩ
r_{on}	Low level output resistance (on state)	I_{OL}= 0.2 mA		1.5	3	kΩ
V_{TH}	Threshold voltage of the control inputs			4.1		V

TYPICAL APPLICATION







1024 - BIT STATIC RANDOM ACCESS MEMORY

- POWER SUPPLY V_{CC}= 5V
- TTL COMPATIBLE ALL INPUTS AND OUTPUTS
- THREE-STATE OUTPUT
- INPUTS PROTECTED AGAINST STATIC CHARGE
- ORGANIZATION 1024 x 1 BIT IN 16 PIN STD PACKAGE

TYPE	STANDBY PWR (mW)	OPERATING PWR (mW)	ACCESS TIME (ns)
M 2102 AL - 2	42	342	250
M 2102 AL	35	174	350
M 2102 AL - 4	35	174	450
M 2102 A - 2	–	342	250
M 2102 A	–	289	350
M 2102 A - 4	–	289	450
M 2102 A - 6	–	289	650

The M 2102A is a high speed 1024 word by 1 static N-channel silicon-gate MOS RAM. The device is fully static and therefore does not require clocks or refreshing to operate. The data is read out non destructively and has the same polarity as the input data.
A low standby power version (M 2102 AL) is also available. It has all the same operating characteristics of the M 2102A with the added feature of 35 mW maximum power dissipation in standby and 174 mW in operations. The device is available in 16 lead dual in-line ceramic package, metal-seal or frit-seal and plastic package.

ABSOLUTE MAXIMUM RATINGS

V_i*	Input voltage (at any pin)	-0.5 to 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature under bias	0 to 70	°C

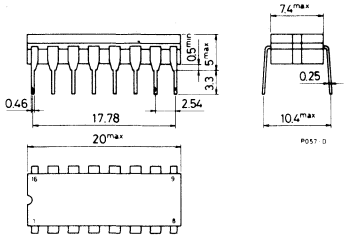
* All voltage are referred to GND pin voltage

ORDERING NUMBERS:
M 2102A - B1 for dual-in-line plastic package
M 2102A - D1 for dual-in-line ceramic package, metal-seal
M 2102A - F1 for dual-in-line ceramic package, frit-seal
M 2102AL - B1 for dual-in-line plastic package
M 2102AL - D1 for dual-in-line ceramic package, metal-seal
M 2102AL - F1 for dual-in-line ceramic package, frit-seal

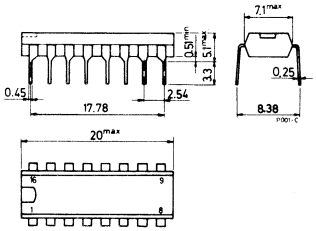
M 2102A
M 2102AL

MECHANICAL DATA (dimensions in mm)

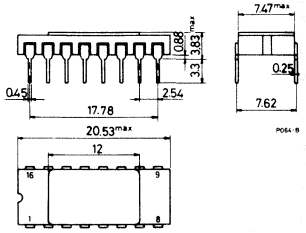
Dual in-line ceramic package frit-seal for M2102A/AL-F1



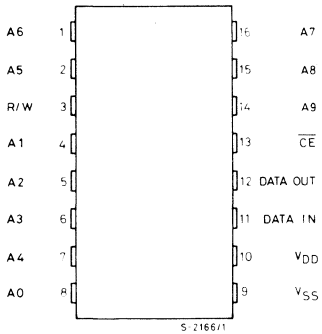
Dual in-line plastic package for M 2102A/AL-B1



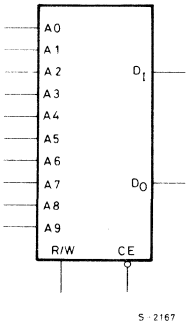
Dual in-line ceramic package metal-seal for M 2102A/AL-D1



PIN CONNECTIONS



LOGIC DIAGRAM



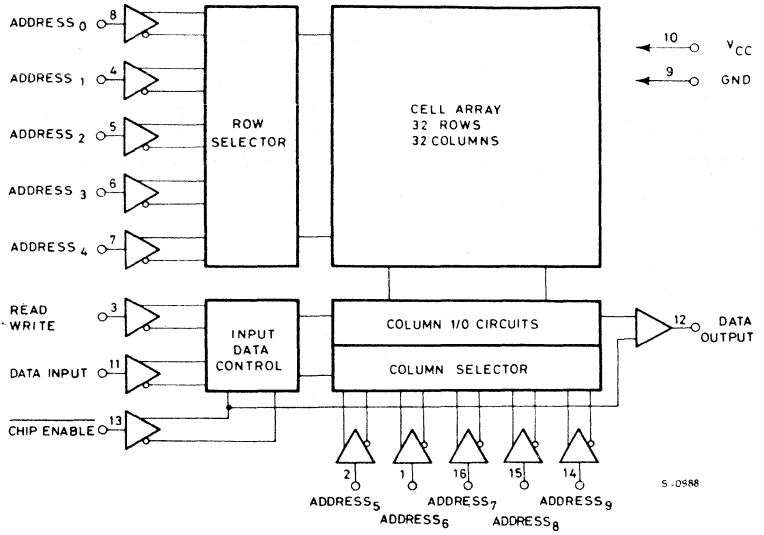
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+5V)

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (V_{CC}= 4.75 to 5.25V, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions	M 2102 A M 2102 AL M 2102 A -4 M 2102 AL-4			M 2102 A -2 M 2102 AL-2			M 2102 A-6			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
V_{IH}	Input high voltage		2		V_{CC}	2		V_{CC}	2.2		V_{CC}	V
V_{IL}	Input low voltage		-0,5		0.8	-0.5		0.8	-0.5		0.65	V
V_{OH}	Output high voltage	I_{OH}= -100 µA	2.4			2.4			2.2			V
V_{OL}	Output low voltage	I_{OL}= 2.1 mA			0.4			0.4			0.45	V
I_{LI}	Input load current	V_I= 0 to 5.25V		1	10		1	10		1	10	µA
I_{OH}	Output leakage current	$\overline{CE}$= 2V. V_O= V_{OH}		1	5		1	5		1	5	µA
I_{OL}	Output leakage current	$\overline{CE}$= 2V V_O= 0.4V		-1	-10		-1	-10		-1	-10	µA
I_{CC}	Supply current	V_I= 5.25V T_{amb}= 0°C Data out open		33	**		45	65		33	55	mA

* Typical values for T_{amb}= 25°C and nominal supply voltage.
** The maximum I_{CC} value is 55 mA for the M 2102A and M 2102A-4, and 33 mA for the M 2102AL and M 2102AL-4.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0 to 70°C, V_{CC}= 5V ± 5% unless otherwise specified)

Parameter		Test condition	M 2102 A -2 M 2102 AL-2		M 2102 A - M 2102 AL		M 2102 A -4 M 2102 AL-4		M 2102 A-6		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
t_{rc}	Read cycle	t_R, t_F= 10 ns Load = 1 TTL gate and C_L= 100 pF	250		350		450		650		ns
t_a	Access time			250		350		450		650	ns
t_E	CE to output time			130		180		230		400	ns
t_{OH1}	Previous read data valid with respect to address		40		40		40		50		ns
t_{OH2}	Previous read data valid with respect to chip enable		0		0		0		0		ns
Write Cycle											
t_{WC}	Write cycle	t_R, t_F= 10 ns Load = 1 TTL gate and C_L= 100 pF	250		350		450		650		ns
t_{AW}	Address to with setup time		20		20		20		200		ns
t_{WP}	Write pulse width		180		250		300		400		ns
t_{WR}	Write recovery time		0		0		0		50		ns
t_S	Data setup time		180		250		300		450		ns
t_h	Data hold time		0		0		0		20		ns
t_{CW}	Chip enable to write setup time		180		250		300		550		ns

CAPACITANCES (T_{amb}= 25°C, f= 1 MHz)

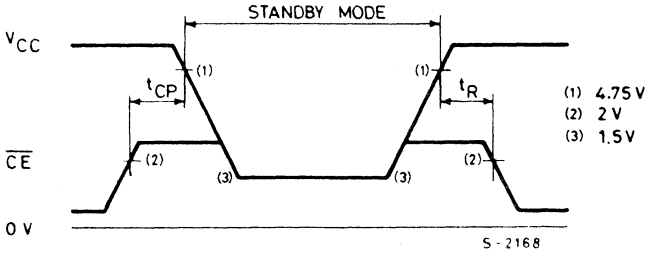
Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	V_I = 0V		3	5	pF
C_o	Output capacitance	V_o = 0V		7	10	pF

STANDBY CHARACTERISTICS (T_{amb} = 0°C to 70°C)

Parameter		Test conditions	M 2102 AL-4 M 2102 AL			M 2102 AL-2			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
V_{PD}	V_{CC} in standby		1.5			1.5			V
V_{CES}**	CE bias in standby	$2V \leqslant V_{PD} \leqslant V_{CC}$ Max.	2			2			V
		$1.5V \leqslant V_{PD} < 2V$	V_{PD}			V_{PD}			V
I_{PD1}	Standby current	All inputs = V_{PD1} = 1.5V		15	23		20	28	mA
I_{PD2}	Standby current	All inputs = V_{PD2} = 2V		20	30		25	38	mA
t_{CP}	Chip deselect to standby time		0			0			ns
t_R***	Standby recovery time		t_{RC}			t_{RC}			ns

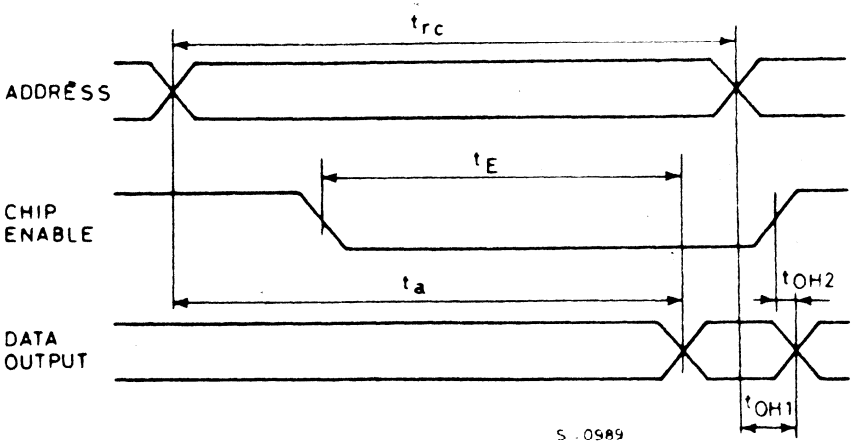
* Typical values are for T_{amb} = 25°C.
** Consider the test conditions as shown: if the standby voltage (V_{PD}) is between 5.25V (V_{CC} max) and 2V, then $\overline{CE}$ must be held at 2V Min. (V_{IH}). If the standby voltage is than 2V but greater than 1.5V (V_{PD} min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
*** $t_R = t_{RC}$ (READ CYCLE TIME).

STANDBY WAVEFORMS

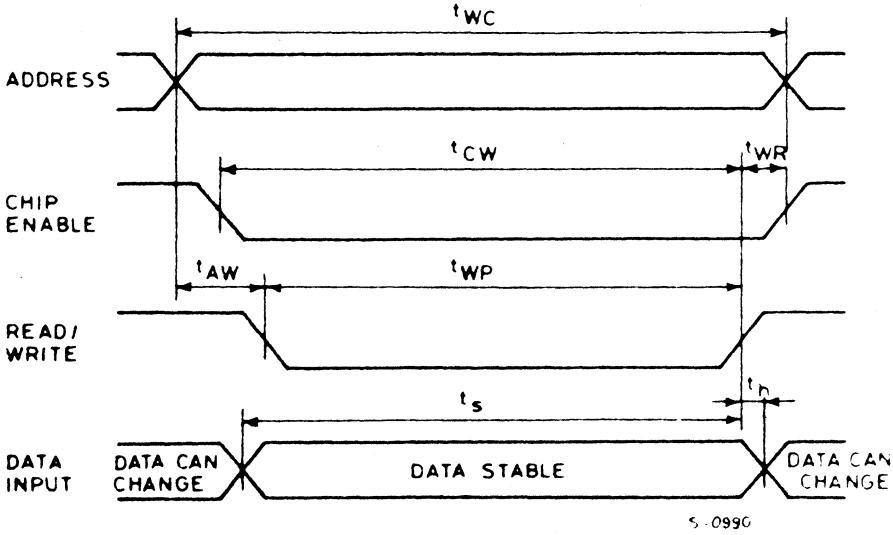


WAVEFORMS

Read cycle



Write cycle



MOS INTEGRATED CIRCUIT

M 2114

PRELIMINARY DATA

1024 x 4 BIT STATIC RAM

- SINGLE +5V SUPPLY
- IDENTICAL CYCLE AND ACCESS TIMES
- COMPLETELY STATIC MEMORY-NO CLOCK OR TIMING STROBE REQUIRED
- DIRECTLY TTL COMPATIBLE: ALL INPUTS AND OUTPUTS
- COMMON DATA INPUT AND OUTPUT USING THREE-STATE OUTPUTS
- HIGH DENSITY 18 PIN PACKAGE

M2114	M2114-2	M2114-3	M2114	M2114L2	M2114L3	M2114L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Current (mA)	100	100	100	70	70	70

The M2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided. The M2114 is designed for memory applications where high performance and high reliability, low cost, large bit storage, and simple interfacing are important design objectives. The M2114 is placed in an 18-pin package for the highest possible density. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

ABSOLUTE MAXIMUM RATINGS*

V_i	Voltage on any pin with respect to ground	3.5 to +7	V
P_{tot}	Total power dissipation	1	W
I_{out}	D.C. output current	5	mA
T_{amb}	Ambient temperature under bias	-10 to 80	°C
T_{stg}	Storage temperature range	-65 to 150	°C

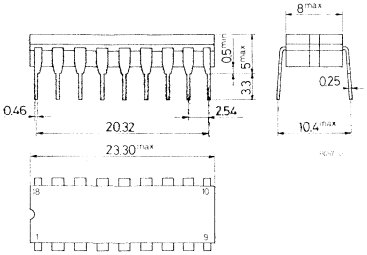
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS: M2114
M2114-2
M2114-3
M2114L
M2114L2
M2114L3
add suffix F1 for frit-seal ceramic DIP or B1 for plastic DIP.

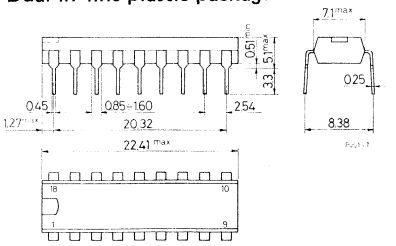
M 2114

MECHANICAL DATA (dimensions in mm)

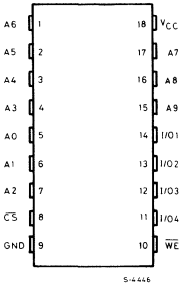
Dual in-line ceramic package, frit seal



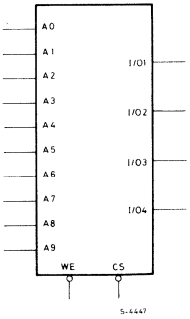
Dual in-line plastic package



PIN CONNECTIONS



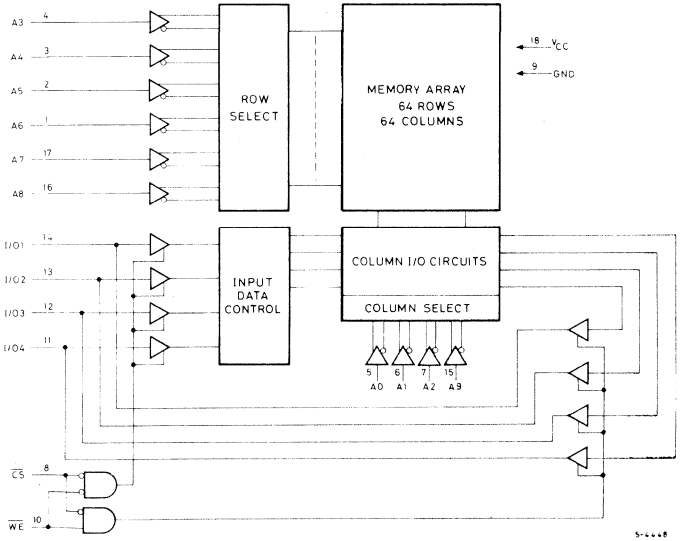
LOGIC DIAGRAM



PIN NAMES

A0–A9	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND GROUND
$\overline{CS}$	CHIP SELECT	
I/O1–I/O4	DATA INPUT/OUTPUT	

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(T_{amb}= 0°C to 70°C, V_{CC}= 5V ± 5%, unless otherwise noted)

Parameter		Test conditions	2114-2, 2114-3, 2114			2114L2, 2114L3, 2114L			Unit
			Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	
I_{LI}	Input Load Current (All Input Pins)	V_I= 0 to 5.25V			10			10	µA
$\|I_{LO}\|$	I/O Leakage Current	$\overline{CS}$= 2.4V, $V_{I/O}$= 0.4V to V_{CC}			10			10	µA
I_{CC1}	Power Supply Current	V_I= 5.25V, $I_{I/O}$= 0 mA, T_{amb}= 25°C		80	95			65	mA
I_{CC2}	Power Supply Current	V_I= 5.25V, $I_{I/O}$= 0 mA, T_{amb}= 0°C			100			70	mA
V_{IL}	Input Low Voltage		-0.5		0.8	-0.5		0.8	V
V_{IH}	Input High Voltage		2.0		6.0	2.0		6.0	V
I_{OL}	Output Low Current	V_{OL}= 0.4V	2.1	6.0		2.1	6.0		mA
I_{OH}	Output High Current	V_{OH}= 2.4V	-1.0	-1.4		-1.0	-1.4		mA
I_{OS}(2)	Out. Short Circuit Current				40			40	mA

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_{amb}= 0°C to 70°C, V_{CC}= 5V ± 5%, unless otherwise noted)

Parameter		2114-2, 2114L2		2114-3, 2114L3		2114, 2114L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE (3)								
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{CO}	Chip Selection to Output Valid		70		100		120	ns
t_{CX}	Chip Selection to Output Active	20		20		20		ns
t_{OTD}	Output 3-state from Deselection		60		80		100	ns
t_{OHA}	Output Hold from Address Change	50		50		50		ns
WRITE CYCLE (4)								
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTW}	Output 3-state from Write		60		80		100	ns
t_{DW}	Data to Write Time Overlap	120		150		200		ns
t_{DH}	Data Hold From Write Time	0		0		0		ns

CAPACITANCES(5) (T_{amb}= 25°C, f = 1.0 MHz)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$= 0V			5	pF
C_I	Input Capacitance	V_I = 0V			5	pF

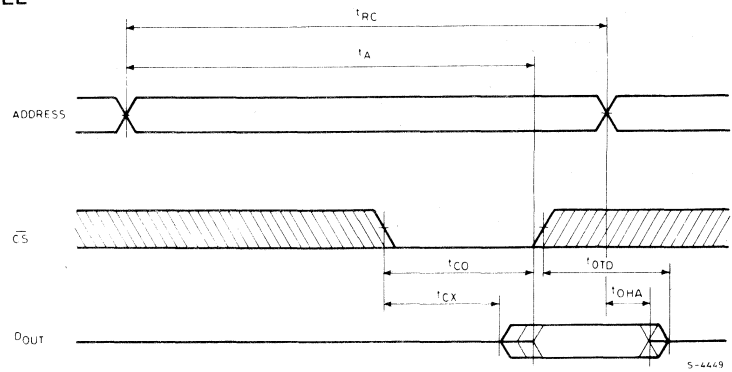
Notes: 1. Typical values are for T_{amb}= 25°C and V_{CC}= 5.0V.
2. Duration not to exceed 30 seconds.
3. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
4. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
5. This parameter is periodically sampled and not 100% tested.

A.C. TEST CONDITIONS

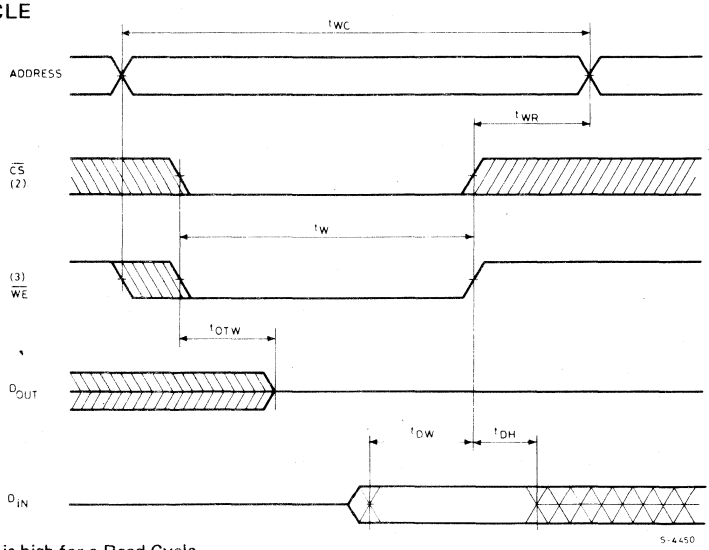
Input Pulse Levels for M2114 = 0.8V to 2.4V
Input Rise and Fall Times = 10 ns
Input and Output Timing Levels = 1.5V
Output Load = 1 TTL Gate and C_L = 100 pF

WAVEFORMS

READ CYCLE (1)



WRITE CYCLE



Notes: 1. $\overline{WE}$ is high for a Read Cycle.
2. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
3. $\overline{WE}$ must be high during all address transitions.

MOS INTEGRATED CIRCUIT

M 2316E

16384 BIT READ ONLY MEMORY

- SINGLE +5V ± 10% POWER SUPPLY
- ACCESS TIME 450 ns (MAX.)
- INPUTS AND OUTPUTS TTL COMPATIBLE
- THREE PROGRAMMABLE CHIP SELECTS FOR SIMPLE MEMORY EXPANSION AND SYSTEM INTERFACE
- COMPLETELY STATIC OPERATION
- THREE-STATE OUTPUT FOR DIRECT BUS INTERFACE

The M 2316E is a 16384 bit static Read Only Memory N-channel Si-Gate MOS organized as 2048 words by 8 bits. Its high bit density is ideal for large, non-volatile data storage applications such as program storage. The three-state outputs and TTL input/output levels allow for direct interface with common system bus structures.
The M 2316E is available in 24-lead dual-in-line plastic package.

ABSOLUTE MAXIMUM RATINGS

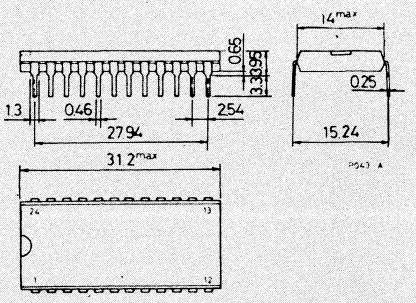
V_i*	Input voltage (at any pin)	-0.5 to 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature	-55 to +125	°C
T_{op}	Operating temperature under bias	-10 to 80	°C

* This voltage is with respect to Ground

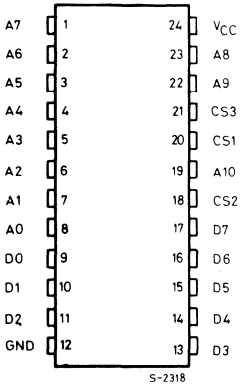
ORDERING NUMBER: M 2316E B1 for dual in-line plastic package

MECHANICAL DATA

Dimensions in mm



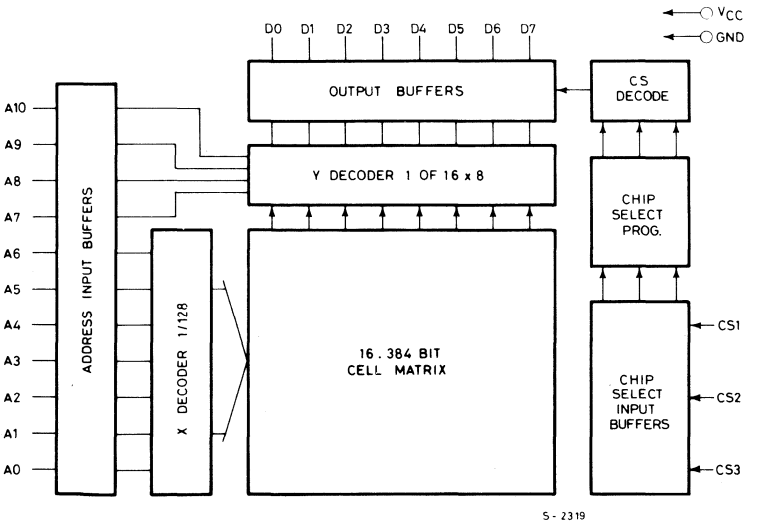
PIN CONNECTIONS



PIN NAMES

A0 - A10	ADDRESS INPUTS
D0 - D7	DATA OUTPUTS
CS1 - CS3	CHIP SELECT INPUTS

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0°C to +70°C, V_{CC}= 5V ± 10% unless otherwise specified)

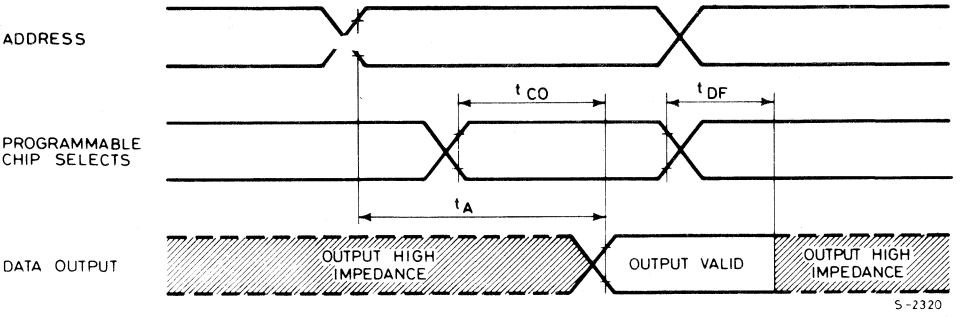
Parameter		Test conditions	Min.	Typ.(1)	Max.	Unit
I_{LI}	Input load current(All input pins)	V_I= 0 to 5.25V			10	μA
I_{LOH}	Output leakage current	Chip deselected V_O= 4V			10	μA
I_{LOL}	Output leakage current	Chip deselected V_O= 0.4V			-20	μA
I_{CC}	Power supply current	All inputs 5.25V Data out open		70	120	mA
V_{IL}	Input low voltage		-0.5		0.8	V
V_{IH}	Input high voltage		2.4		V_{CC}+1V	V
V_{OL}	Output low voltage	I_{OL}= 2.1 mA			0.4	V
V_{OH}	Output high voltage	I_{OH}= -400 μA	2.4			V

Note: 1 Typical values for T_{amb}= 25°C and nominal supply voltage.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0°C to 70°C, V_{CC}= +5V ± 10%unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
t_A	Address to output delay time	Output load = 1 TTL gate and C_L= 100 pF Input pulse levels -0.8 to 2.4V Input pulse rise and fall times (10% to 90%) -20 ns Timing Measurement Reference level: Input = 1V and 2.2V Output = 0.8V and 2.2V			450	ns
t_{CO}	Chip select to output enable delay time				120	ns
t_{DF}	Chip deselect to output data float delay time		10		100	ns
C_I	Input capacitance	T_{amb}= 25°C f = 1 MHz All pins except pin under test tied to AC ground		5	10	pF
C_O	Output capacitance	T_{amb}= 25°C f = 1 MHz All pins, except pin under test tied to AC ground		10	15	pF

A.C. Waveforms



MOS INTEGRATED CIRCUIT

M 2716

PRELIMINARY DATA

16K (2K x 8) UV ERASABLE PROM

- FAST ACCESS TIME : 350 ns MAX. M2716-1
  450 ns MAX. M2716
- SINGLE +5V POWER SUPPLY
- LOW POWER DISSIPATION : 525 mW MAX. ACTIVE POWER
  132 mW MAX. STANDBY POWER
- SIMPLE PROGRAMMING REQUIREMENTS
  – SINGLE LOCATION PROGRAMMING
  – PROGRAMS WITH ONE 50 ms PULSE
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING READ AND PROGRAM
- COMPLETELY STATIC

The M2716 is a 16.384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The M2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.
The M2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Z80 and Z8000.
The M2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.
The M2716 has the simplest and fastest method yet devised for programming EPROMs — single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time-either individually, sequentially or at random, with the M2716's single address location programming. Total programming time for all 16.384 bits is only 100 seconds.

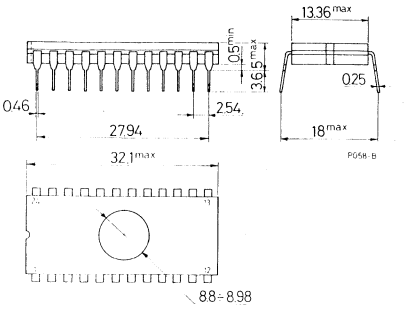
ABSOLUTE MAXIMUM RATINGS*

	All input or output voltages with respect to ground	+6 to -0.3	V
V_{pp}	Supply voltage with respect to ground during program	+26.5 to -0.3	V
T_{amb}	Ambient temperature under bias	-10 to +80	°C
T_{stg}	Storage temperature range	-65 to +125	°C

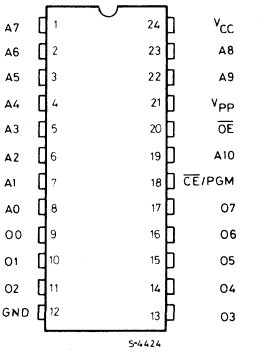
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS: M2716F1 for frit-seal dual in-line ceramic package
M2716-1F1 for frit-seal dual in-line ceramic package

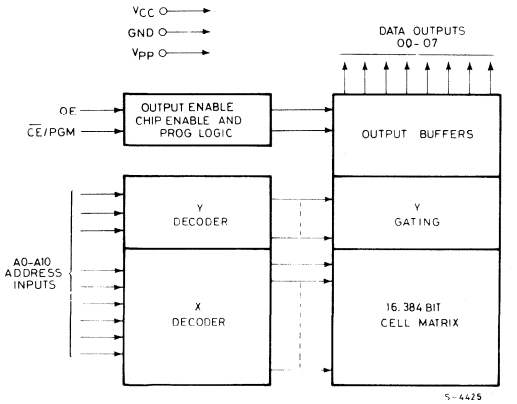
MECHANICAL DATA (dimensions in mm)



PIN CONNECTIONS



BLOCK DIAGRAM



PIN NAMES

A0–A10	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O0–O7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

Note:
The five modes of operation of the M2716 are listed in this table. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

READ OPERATION

D.C. AND A.C. OPERATING CONDITIONS

	M2716	M2716-1
Temperature range	0°C–70°C	0°C–70°C
V_{CC} Power Supply (1,2)	5V ± 5%	5V ± 10%
V_{PP} Power Supply (2)	V_{CC}	V_{CC}

D.C. AND OPERATING CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.(3)	Max.	
I_{LI}	Input Load Current	V_I = 5.25V			10	μA
I_{LO}	Output Leakage Current	V_O = 5.25V			10	μA
I_{PP1} (2)	V_{PP} Supply Current	V_{PP} = 5.25V			8	mA
I_{CC1} (2)	V_{CC} Supply Current (Standby)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}		10	25	mA
I_{CC2} (2)	V_{CC} Supply Current (Active)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}		57	100	mA
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 μA	2.4			V

A.C. CHARACTERISTICS

Parameter		Test conditions	M2716		M2716-1		Unit
			Min.	Max.	Min.	Max.	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		450		350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		450		350	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$ = V_{IL}		120		120	ns
t_{DF}	Output Enable High to Output Float	$\overline{CE}$ = V_{IL}	0	100	0	100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		ns

CAPACITANCE (4) (T_{amb} = 25°C, f = 1 MHz)

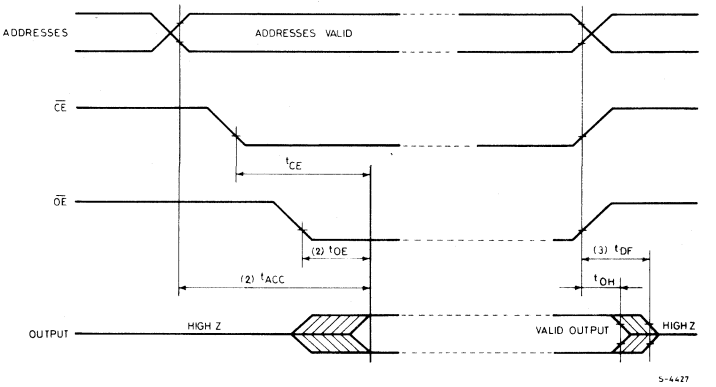
Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	V_I = 0V		4	6	pF
C_O	Output capacitance	V_O = 0V		8	12	pF

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_{amb} = 25°C and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.

A.C. TEST CONDITIONS:

Output load : 1 TTL gate and C_L = 100 pF.
Input Rise and Fall Times : ⩽ 20 ns
Input Pulse levels : 0.8V to 2.2V
Timing Measurement Reference Level : Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. WAVEFORMS (1)



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of CE without impact on t_{ACC}.
3. t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

READ MODE

The M2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

STANDBY MODE

The M2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The M2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because M2716's are usually used in larger memory arrays, the product has 2 line control function that accomodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING OPERATION [1] (T_{amb} = 25°C ± 5%, V_{CC} [2] = 5V ± 5%, V_{PP} [2,3] = 25V ± 1V)

D.C. AND OPERATING CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (for Any Input)	V_I = 5.25V/0.45			10	µA
I_{PP1}	V_{PP} Supply Current	$\overline{CE}$/PGM = V_{IL}			8	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}$/PGM = V_{IH}			30	mA
I_{CC}	V_{CC} Supply Current				100	mA
V_{IL}	Input Low Level		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC}+1	V

A.C. CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		2			µs
t_{OEH}	$\overline{OE}$ Hold Time		2			µs
t_{DH}	Data Hold Time		2			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}$/PGM = V_{IL}	0		120	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}$/PGM = V_{IL}			120	ns
t_{PW}	Program Pulse Width		45	50	55	ms
t_{PRT}	Program Pulse Rise Time		5			ns
t_{PFT}	Program Pulse Fall Time		5			ns

CAUTION: The V_{CC} and V_{PP} supplied must be sequenced on and off such that V_{CC} is applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} to prevent damage to the M2716. The maximum allowable voltage during programming which may be applied to the V_{PP} with respect to ground is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding the 26-volt maximum specification. For convenience in programming, the M2716 may be verified with the V_{PP} supply at 25V ±1V. During normal read operation, however, V_{PP} must be at V_{CC}.

Notes: 1. SGS-ATES guarantees the product only if it is programmed to specifications described herein.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The M2716 must not be inserted into or removed from a board with V_{PP} at 25 ± 1V to prevent damage to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

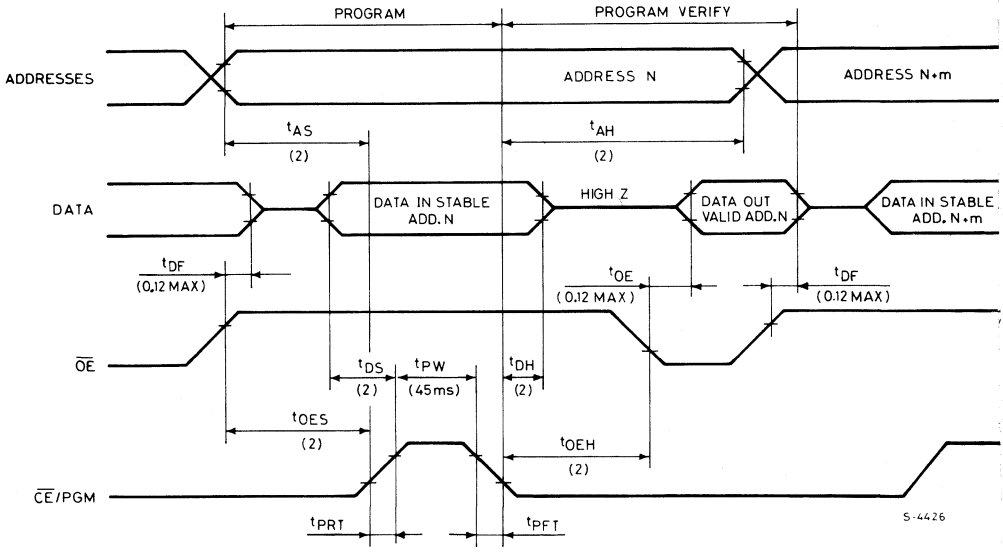
A.C. TEST CONDITIONS

V_{CC} = 5V ± 5%
V_{PP} = 25V ± 1V
Input Rise and Fall Times (10% to 90%) = 20 ns

Input Pulse Levels = 0.8V to 2.2V
Input Timing Reference Level = 1V and 2V
Output Timing Reference Level = 0.8V and 2V

PROGRAMMING WAVEFORMS

(V_{PP} = 25V ± 1V, V_{CC} = 5V ± 5%)



Note: All times shown in parentheses are minimum times and are μsec unless otherwise noted.

PROGRAMMING

Initially, and after each erasure, all bits of the M2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The M2716 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple M2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input-programs the paralleled M2716s.

PROGRAM INHIBIT

Programming of multiple M2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel M2716s may be common. A TTL level program pulse applied to a M2716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that M2716. A low level $\overline{CE}$/PGM input inhibits the other M2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

ERASURE OPERATION

The erasure characteristics of the M2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical M2716 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M2716 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested to put opaque labels over the M2716 window to prevent unintentional erasure.

The recommended erasure procedure for the M2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e. UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The M2716 should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

MOS INTEGRATED CIRCUIT

M 4015

PRELIMINARY DATA

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

- POWER SUPPLY V_{DD}= 12V, V_{CC}= 5V, V_{BB}= -5V (ALL WITH ± 10% TOLERANCE EXCEPT V_{DD} ± 5)
- ALL INPUTS ARE LOW CAPACITANCE AND TTL COMPATIBLE
- INPUT LATCHES FOR ADDRESSES, CHIP SELECT AND DATA IN
- INPUTS PROTECTED AGAINST STATIC CHARGE
- THREE-STATE TTL COMPATIBLE OUTPUT
- OUTPUT DATA LATCHED AND VALID INTO NEXT CYCLE
- ECL. COMPATIBLE ON V_{BB} POWER SUPPLY (-5.7V)
- LOW POWER CONSUMPTION: ACTIVE POWER UNDER 470 mW
  STANDBY POWER UNDER 27 mW
- ORGANIZATION 4096 x 1 BIT IN 16-PIN STD PACKAGE
- FUNCTIONAL AND PIN COMPATIBLE WITH MK4027
- ACCESS TIME: TYPE M4015 250 ns

The M4015 is a 4096 word by 1 bit dynamic N-channel silicon gate MOS RAM. The M4015 uses a single transistor cell utilizing a dynamic storage technique and dynamic control circuitry with low power dissipation. A unique multiplexing and latching technique for the address inputs permits the M4015 to be mounted in a standard 16-pin package. The M4015 incorporates several flexible operating modes. In addition to the usual read and write cycles, read modify write, page mode and RAS-only refresh cycles are available with the M4015. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA). The device is available in 16-lead dual in-line plastic or ceramic package (metal-seal), and ceramic package (frit-seal).

ABSOLUTE MAXIMUM RATINGS*

	Voltage on any pin relative to V_{BB}	-0.5 to +20	V
	Voltage on V_{DD}, V_{CC} relative to V_{SS}	-1 to +15	V
	V_{BB}-V_{SS} (V_{DD}-$V_{SS} > 0$)	0	V
T_{op}	Operating temperature	0 to +55	°C
T_{stg}	Storage temperature for ceramic package	-65 to +150	°C
	for plastic package	-55 to +125	°C
I_o	Short circuit output current	50	mA
P_{tot}	Total power dissipation	1	W

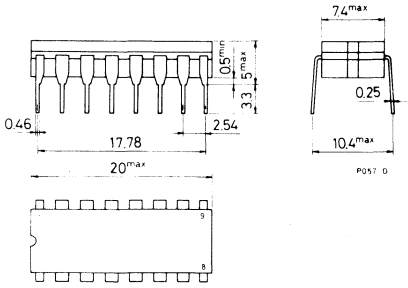
* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBER: M4015 F1 for dual in-line ceramic package, frit-seal

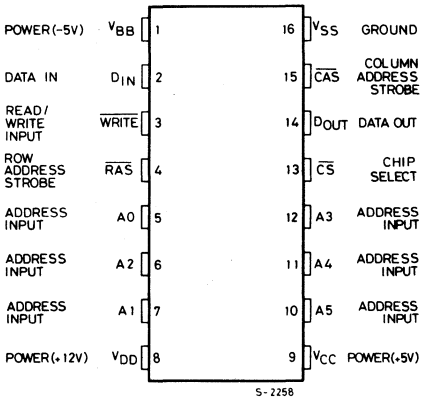
M 4015

MECHANICAL DATA (dimensions in mm)

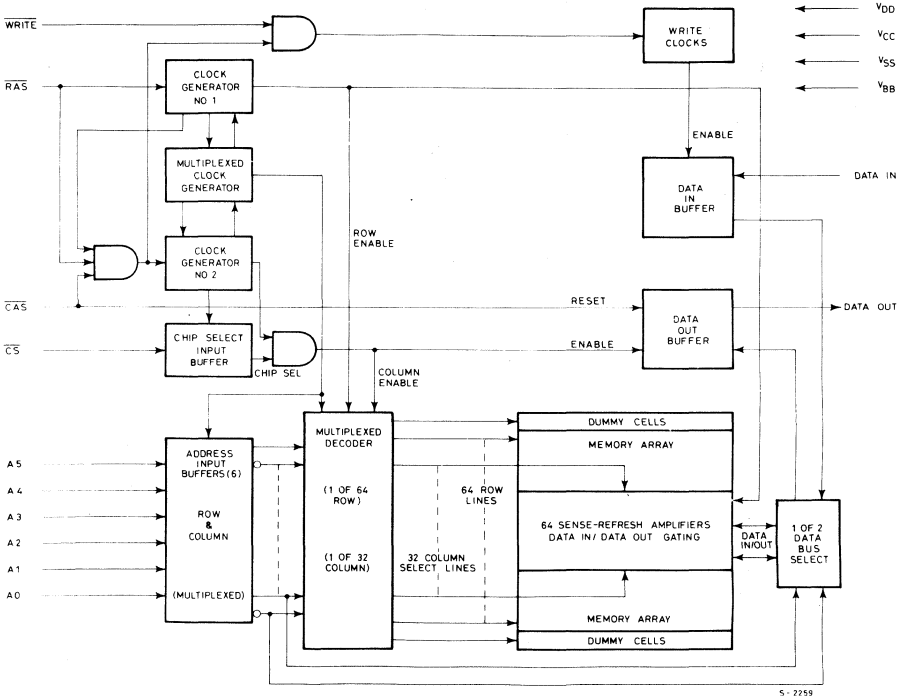
Dual in-line ceramic package frit-seal
for M4015 F1



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS[1] (T_{amb}= 0 to 55°C)[4]

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply voltage	11.4	12	12.6	V	2
V_{CC}	Supply voltage	4.5	5	5.5	V	2, 3
V_{SS}	Supply voltage	0	0	0	V	2
V_{BB}	Supply voltage	-4.5	-5	-5.7	V	2
V_{IHC}	Input high voltage on $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	3		7	V	2
V_{IH}	Input high voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	3		7	V	2
V_{IL}	Input low voltage, all inputs	-1		0.65	V	2

DC ELECTRICAL CHARACTERISTICS[1] (T_{amb}= 0 to 55°C)[4] (V_{DD}= 12V ± 5% , V_{CC}= 5V ± 10% , V_{SS}= 0V, V_{BB}= -5.7 to -4.5V)

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
I_{DD1}	Average V_{DD} power supply current			35	mA	5
I_{DD2}	Standby V_{DD} power supply current		3		mA	8
I_{DD3}	Average V_{DD} power supply current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} power supply current				mA	6
I_{BB}	Average V_{BB} power supply current			150	µA	
$I_{I(L)}$	Input leakage current (any input)			10	µA	7
$I_{O(L)}$	Output leakage current			10	µA	8, 9
V_{OH}	Output high voltage (I_{SOURCE}= -5 mA)	2.4			V	
V_{OL}	Output low voltage (I_{SINK}= 3.2 mA)			0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[1,10,15]

(T_{amb} = 0 to 55°C)[4], (V_{DD} = 12V ± 5% , V_{CC} = 5V ± 10% , V_{SS} = 0V, V_{BB} = -5.7 to -4.5V)

Parameter		M4015			Unit	Notes
		Min.	Typ.	Max.		
t_{RC}	Random read or write cycle time	380			ns	
t_{RWC}	Read write cycle time	395			ns	
t_{RMW}	Read modify write cycle time	470			ns	
t_{RAC}	Access time from row address strobe			250	ns	11-13
t_{CAC}	Access time from column address strobe			165	ns	12-13
t_{OFF}	Output buffer turn-off delay			60	ns	
t_{RP}	Row address strobe precharge time	120			ns	
t_{RAS}	Row address strobe pulse width	250		4000	ns	
t_{RSH}	Row address strobe hold time	165			ns	
t_{CAS}	Column address strobe pulse width	165			ns	
t_{CSH}	Column address strobe hold time	250			ns	
t_{RCD}	Row to column strobe delay	35		85	ns	14
t_{ASR}	Row address set-up time	0			ns	
t_{RAH}	Row address hold time	35			ns	
t_{ASC}	Column address set-up time	0			ns	
t_{CAH}	Column address hold time	75			ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	160			ns	
t_{CSC}	Chip select set-up time	0			ns	
t_{CH}	Chip select hold time	75			ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	160			ns	
t_T	Transition time (rise and fall)	5		50	ns	15
t_{RCS}	Read command set-up time	0			ns	
t_{RCH}	Read command hold time	0			ns	
t_{WCH}	Write command hold time	75			ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	160			ns	
t_{WP}	Write command pulse width	75			ns	
t_{RWL}	Write command to row strobe lead time	100			ns	
t_{CWL}	Write command to column strobe lead time	100			ns	
t_{DS}	Data in set-up time	0			ns	16
t_{DH}	Data in hold-time	75			ns	16

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (cont.)

Parameter		M4015			Unit	Notes
		Min.	Typ.	Max.		
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	160			ns	
t_{CRP}	Column to row strobe precharge time	0			ns	
t_{CP}	Column precharge time	110			ns	
t_{RFSH}	Refresh period			1	ms	
t_{WCS}	Write command set-up time	0			ns	17
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	90			ns	17
t_{RWD}	RAS to WRITE delay	175			ns	17
t_{DOH}	Data out hold time	4			μs	

CAPACITANCES (T_{amb} = 0 to 55°C, V_{DD} = 12V ± 5% ; V_{SS} = 0V; V_{BB} = -5.7 to -4.5V)

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
C_{I1}	Input capacitance (A_0-A_5), D_{IN}, $\overline{CS}$		4	5	pF	18
C_{I2}	Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		8	10	pF	18
C_O	Output capacitance (D_{OUT})		5	7	pF	8-18

1. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
2. All voltage referenced to V_{SS}, V_{BB} must be applied before and removed after other supply voltages.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. T_{amb} is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min).
6. I_{CC} depends on output loading. The V_{CC} supply is connected to the output buffer only.
7. All device pins at 0 volts except V_{BB} which is at -5V and the pin under test which is at +10V.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leq V_{out} \leq +10V$.
10. AC measurements assume $t_T = 5$ ns.
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
12. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
13. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.
18. Effective capacitance is calculated from the equation: $C = \frac{\Delta Q}{\Delta V}$ with $\Delta V = 3$ volts.

MOS INTEGRATED CIRCUIT

M 4027

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

- POWER SUPPLY V_{DD}= 12V, V_{CC}= 5V, V_{BB}= -5V (ALL WITH ± 10% TOLERANCE)
- ALL INPUTS ARE LOW CAPACITANCE AND TTL COMPATIBLE
- INPUT LATCHES FOR ADDRESSES, CHIP SELECT AND DATA IN
- INPUTS PROTECTED AGAINST STATIC CHARGE
- THREE-STATE TTL COMPATIBLE OUTPUT
- OUTPUT DATA LATCHED AND VALID INTO NEXT CYCLE
- ECL COMPATIBLE ON V_{BB} POWER SUPPLY (-5.7V)
- LOW POWER CONSUMPTION: ACTIVE POWER UNDER 470 mW
  STANDBY POWER UNDER 27 mW
- ORGANIZATION 4096 x 1 BIT IN 16-PIN STD PACKAGE
- FUNCTIONAL AND PIN COMPATIBLE WITH MK4027
- ACCESS TIME: TYPE M 4027-2 150 ns
  TYPE M 4027-3 200 ns
  TYPE M 4027-4 250 ns

The M 4027 is a 4096 word by 1 bit dynamic N-channel silicon gate MOS RAM. The M 4027 uses a single transistor cell utilizing a dynamic storage technique and dynamic control circuitry with low power dissipation. A unique multiplexing and latching technique for the address inputs permits the M 4027 to be mounted in a standard 16-pin package. The M 4027 incorporates several flexible operating modes. In addition to the usual read and write cycles, read modify write, page mode and RAS-only refresh cycles are available with the M 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA). The device is available in 16-lead dual in-line plastic or ceramic package (metal-seal), and ceramic package (frit-seal).

ABSOLUTE MAXIMUM RATINGS*

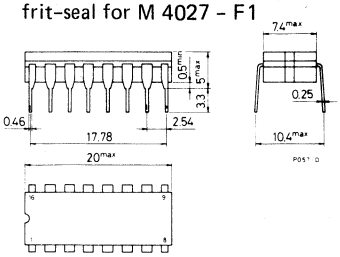
	Voltage on any pin relative to V_{BB}	-0.5 to +20	V
	Voltage on V_{DD}, V_{CC} relative to V_{SS}	-1 to +15	V
	V_{BB}-V_{SS} (V_{DD}-$V_{SS} > 0$)	0	V
T_{op}	Operating temperature	0 to +70	°C
T_{stg}	Storage temperature for ceramic package	-65 to +150	°C
	for plastic package	-55 to +125	°C
I_o	Short circuit output current	50	mA
P_{tot}	Total power dissipation	1	W

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

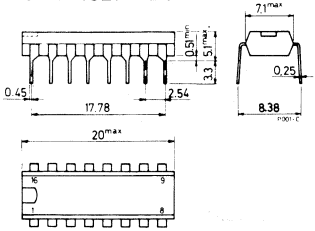
ORDERING NUMBERS: M 4027-2/3/4 B1 for dual in-line plastic package
M 4027-2/3/4 D1 for dual in-line ceramic package, metal-seal
M 4027-2/3/4 F1 for dual in-line ceramic package, frit-seat

MECHANICAL DATA (dimensions in mm)

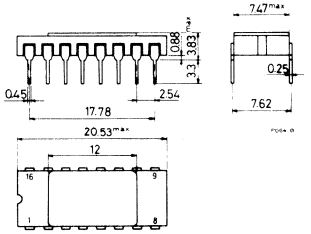
Dual in-line ceramic package
frit-seal for M 4027 - F1



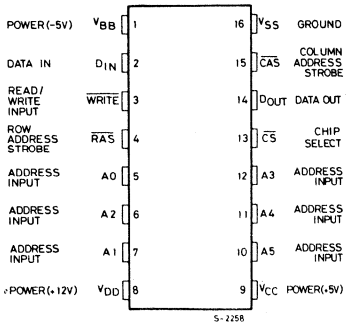
Dual in-line plastic package
for M 4027 - B1



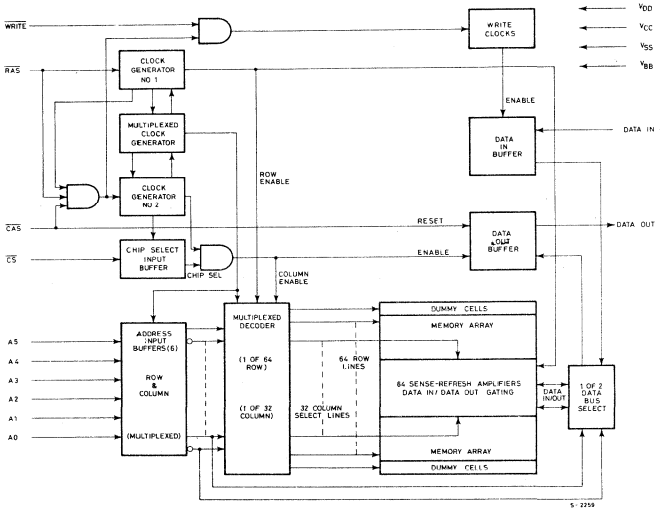
Dual in-line ceramic package
metal-seal for M 4027 - D1



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS[1] (T_{amb}= 0 to 70°C)[4]

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply voltage	10.8	12	13.2	V	2
V_{CC}	Supply voltage	4.5	5	5.5	V	2, 3
V_{SS}	Supply voltage	0	0	0	V	2
V_{BB}	Supply voltage	-4.5	-5	-5.7	V	2
V_{IHC}	Input high voltage on $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7	V	2
V_{IH}	Input high voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7	V	2
V_{IL}	Input low voltage, all inputs	-1		0.8	V	2

DC ELECTRICAL CHARACTERISTICS[1] (T_{amb}= 0 to 70°C)[4] (V_{DD}= 12V ± 10%, V_{CC}= 5V ± 10%, V_{SS}= 0V, V_{BB}= - 5.7 to -4.5V)

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
I_{DD1}	Average V_{DD} power supply current			35	mA	5
I_{DD2}	Standby V_{DD} power supply current			2	mA	8
I_{DD3}	Average V_{DD} power supply current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} power supply current				mA	6
I_{BB}	Average V_{BB} power supply current			150	µA	
$I_{I(L)}$	Input leakage current (any input)			10	µA	7
$I_{O(L)}$	Output leakage current			10	µA	8, 9
V_{OH}	Output high voltage (I_{SOURCE}= -5 mA)	2.4			V	
V_{OL}	Output low voltage (I_{SINK}= 3.2 mA)			0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[1, 10, 15]

(T_{amb} = 0 to 70°C)[4], (V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{SS} = 0V, V_{BB} = -5.7 to -4.5V)

Parameter		Types						Unit	Notes
		M 4027-2		M 4027-3		M 4027-4			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random read or write cycle time	320		375		380		ns	
t_{RWC}	Read write cycle time	320		375		395		ns	
t_{RMW}	Read modify write cycle time	320		405		470		ns	
t_{RAC}	Access time from row address strobe		150		200		250	ns	11-13
t_{CAC}	Access time from column address strobe		100		135		165	ns	12-13
t_{OFF}	Output buffer turn-off delay		40		50		60	ns	
t_{RP}	Row address strobe precharge time	100		120		120		ns	
t_{RAS}	Row address strobe pulse width	150	10000	200	10000	250	10000	ns	
t_{RSH}	Row address strobe hold time	100		135		165		ns	
t_{CAS}	Column address strobe pulse width	100		135		165		ns	
t_{CSH}	Column address strobe hold time	150		200		250		ns	
t_{RCD}	Row to column strobe delay	20	50	25	65	35	85	ns	14
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	-10		-10		-10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CSC}	Chip select set-up time	-10		-10		-10		ns	
t_{CH}	Chip select hold time	45		55		75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_T	Transition time (rise and fall)	3	35	5	50	5	50	ns	15
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to row strobe lead time	50		70		85		ns	
t_{CWL}	Write command to column strobe lead time	50		70		85		ns	
t_{DS}	Data in set-up time	0		0		0		ns	16

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (cont.)

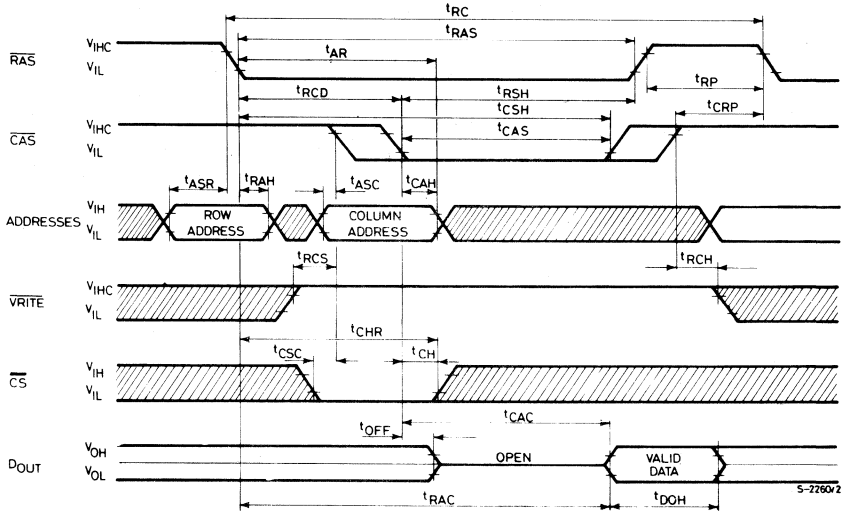
Parameter		Types						Unit	Notes
		M 4027-2		M 4027-3		M 4027-4			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{DH}	Data in hold-time	45		55		75		ns	16
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CRP}	Column to row strobe precharge time	0		0		0		ns	
t_{CP}	Column precharge time	60		80		110		ns	
t_{RFSH}	Refresh period		2		2		2	ms	
t_{WCS}	Write command set-up time	0		0		0		ns	17
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	17
t_{RWD}	RAS to WRITE delay	110		145		175		ns	17
t_{DOH}	Data out hold time	10		10		10		μs	

CAPACITANCES (T_{amb} = 0 to 70°C, V_{DD} = 12V ± 10%; V_{SS} = 0V; V_{BB} = -5.7 to -4.5V)

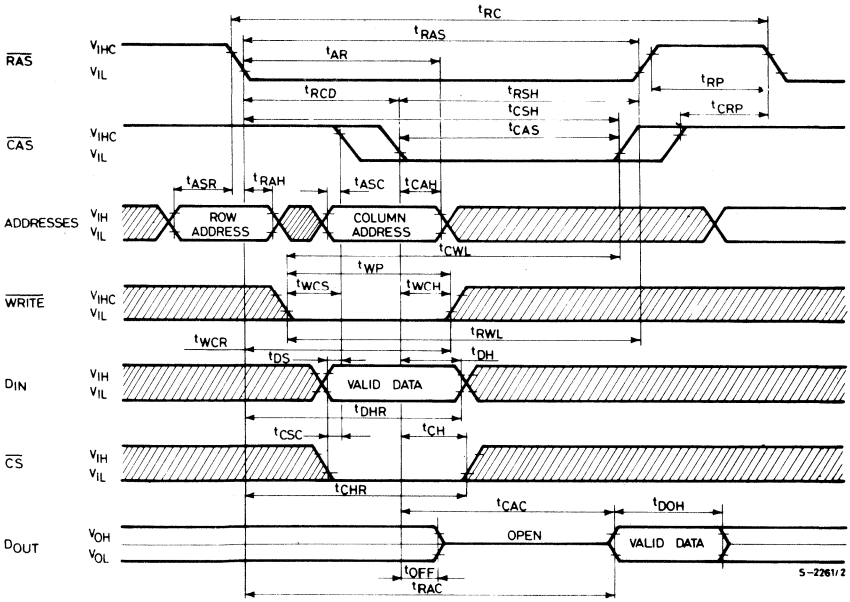
Parameter		Values		Unit	Notes
		Typ.	Max.		
C_{I1}	Input capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	18
C_{I2}	Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	18
C_O	Output capacitance (D_{OUT})	5	7	pF	8-18

1. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
2. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. T_{amb} is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min).
6. I_{CC} depends on output loading. The V_{CC} supply is connected to the output buffer only.
7. All device pins at 0 volts except V_{BB} which is at -5V and the pin under test which is at +10V.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leq V_{out} \leq +10V$.
10. AC measurements assume t_T = 5 ns.
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
12. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
13. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.
18. Effective capacitance is calculated from the equation: $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts.

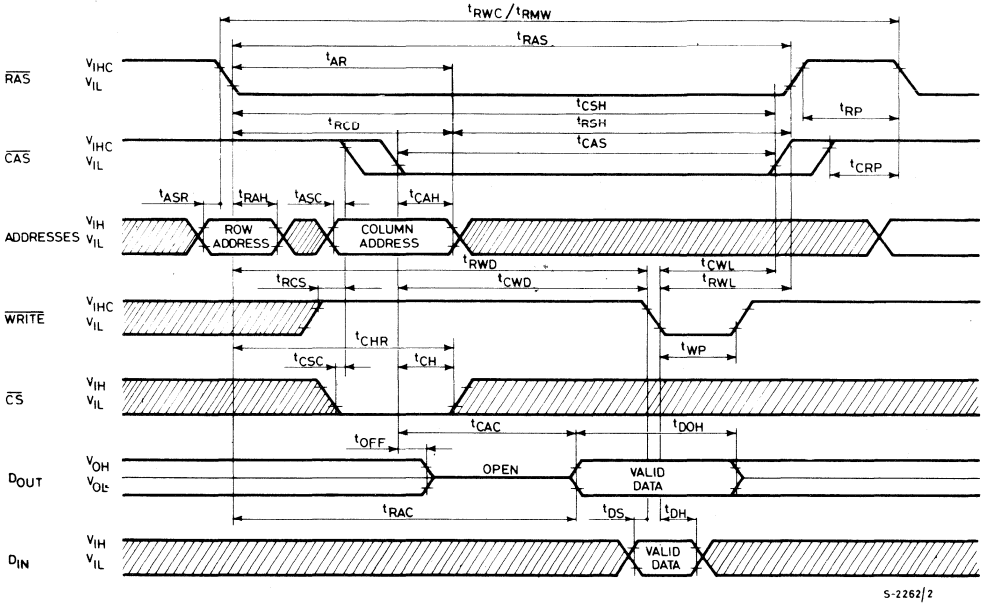
READ CYCLE



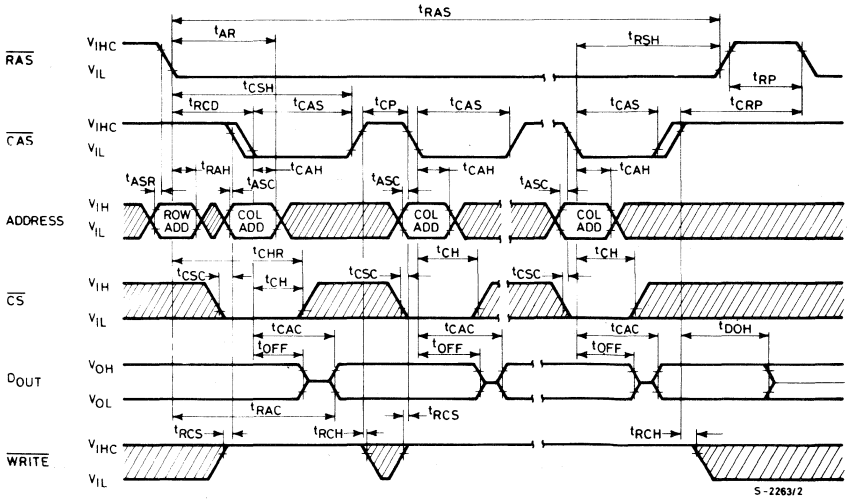
WRITE CYCLE
(early write)



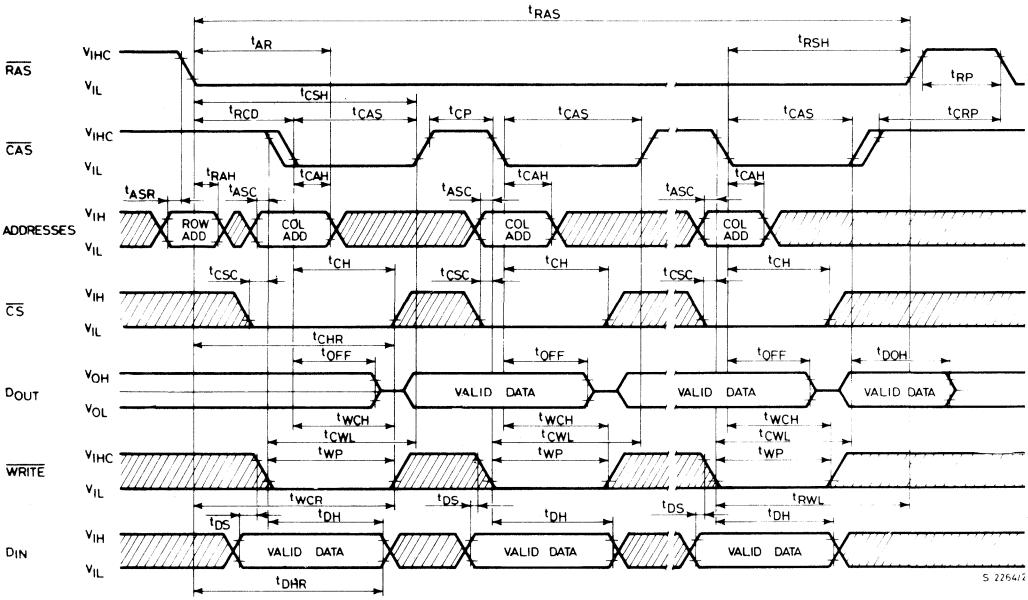
READ WRITE/READ MODIFY-WRITE CYCLE



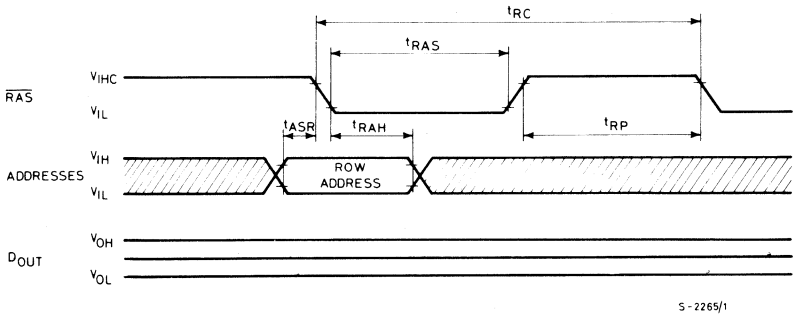
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



RAS ONLY REFRESH CYCLE



ADDRESSING

The 12 address bits required to decode one of 4096 cell locations within the M 4027 are multiplexed onto the 6 address inputs and latched into the on-chip row and column address latches.
Row Address Strobe ($\overline{RAS}$) latches the six row address bits onto the chip. Column Address Strobe ($\overline{CAS}$) latches the six column address bits plus Chip Select ($\overline{CS}$) onto the chip.
Since the internal circuitry allows the columns information to be externally applied to the chip before it is actually required, the hold time requirements for column address and $\overline{CS}$ are also referenced to $\overline{RAS}$. However, this gated $\overline{CAS}$ feature allows the systems designer to compensate for timing skews that may be encountered in the multiplexing operation.
Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.
Additional timing margin is gained because column address is not required until $\overline{CAS}$ makes its negative transition.
The timing is further simplified by the positive transition of $\overline{CAS}$ not being referenced to the positive transition of $\overline{RAS}$. In fact, $\overline{CAS}$ need not go HIGH until the beginning of the next cycle.

DATA INPUT/OUTPUT

Data to be written into selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active.
The later of this signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In into the latch. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is activated prior to $\overline{CAS}$, the Data In is strobe by $\overline{CAS}$, and set-up time and hold time are referenced to $\overline{CAS}$. If the Data In input is not available at $\overline{CAS}$ time or the cycle is a read-write or read-modify-write, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$) Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected. Data is retrieved from the memory in read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

At the beginning of a memory cycle, the state of the Data Out latch and buffer depend on the previous memory cycle.
Changes in the condition of Data Out latch are initiated by $\overline{CAS}$. The negative transition of $\overline{CAS}$ causes the Data Output (D_{OUT}) to unconditionally go to its open-circuit state. If will remain open-circuited until after the access D_{OUT} time, the will assume the proper state for the type of cycle performed.
If the cycle is a read, read-modify-write, or a delayed write and the chip is selected, then the D_{OUT} latch and buffer will contain the data from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then D_{OUT} will contain the input data.
Once the D_{OUT} goes active, it will remain active until the next negative transition of $\overline{CAS}$.
If the cycle is a $\overline{CAS}$ only cycle (no $\overline{RAS}$ signal), then D_{OUT} will assume the open - circuit state.
The same istrue for normal cycles (both $\overline{RAS}$ and $\overline{CAS}$ present-when the chip is unselected D_{OUT} remains in the open-circuit state until the next negative transition of $\overline{CAS}$.
$\overline{RAS}$ only refresh cycles (no $\overline{CAS}$) have no effect on the D_{OUT}.
However, when $\overline{RAS}$ only refresh cycles are continued for extended periods of time, D_{OUT} may eventually go open-circuit.
If the chip unselected, it will not accept a write command and the D_{OUT} will remain in the open-circuit state.

INPUT/OUTPUT LEVELS

All inputs, including the two address strobes, interface directly with TTL.
The high-impedance, low-capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements.
The 3-state output buffer is a low impedance to V_{CC} for a logic "1" and a low impedance to V_{SS} for a logic "0".
The output resistance to V_{CC} (logic "1" state) is 420 ohm maximum and 135 ohm tipically.
The output resistance to V_{SS} (logic "0" state) is 125 ohm maximum and 35 ohm tipically.
The separate V_{CC} pin allows the output buffer to be powered from supply voltage of the logic to which chip is interfaced.
During battery stand-by operation, the V_{CC} pin may be unpowered without effecting the M 4027 refresh operation.
This allows all system logic, except $\overline{RAS}$ timing circuitry and refresh address logic, to be turned off during battery stand-by to save power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row address every two millisecond or less.
Any cycle in which a $\overline{RAS}$ signal occurs, accomplished a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input.
A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.
If, during a refresh cycle, the M 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (when $\overline{RAS}$ is the only signal applied to the chip) are contained for extended periods, the output buffer may eventually lose proper data and go open-circuit.
The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the M 4027 and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle.
Tipically, the power is 170 mW at 1 μsec cycle rate for M 4027 with a worse case power of less than 470 mW at 320 μsec cycle time.
To reduce the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips.
The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output).
Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs.
If the $\overline{RAS}$ signal is decoded and supplied only the selected chips, then the chip select ($\overline{CS}$) input of all chips can be at a logic 0.
Then chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input.
For refresh cycles, however, either the $\overline{CS}$ input for all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR" outputs from turning on with opposing force. Note that the M 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page mode" feature of the M 4027 allows for successive memory operations at multiple column location of the same row address with increased speed without an increase in power.
This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at logic 0 throughout all successive memory cycles in which the row address is common.
This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. The time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page made cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles.
This feature allows the page boundary to be extended beyond the 64 column location in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and deconding $\overline{CS}$ to select the proper block.

POWER UP

The M 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, SGS-ATES recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.
Under system failure condiction in which one or more supplied exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state. After power is applied to the device, the M 4027 requires several cycles before proper device operation is achieved.
Any 8 cycles which perform refresh are adequate for this purpose.

MOS INTEGRATED CIRCUIT

M 4116

16384-BIT DYNAMIC RANDOM ACCESS MEMORY

- RECOGNIZED INDUSTRY STANDARD 16-PIN CONFIGURATION
- 150ns ACCESS TIME, 320ns CYCLE (M 4116-2)
  200ns ACCESS TIME, 375ns CYCLE (M 4116-3)
  250ns ACCESS TIME, 410ns CYCLE (M 4116-4)
- ± 10% TOLERANCE ON ALL POWER SUPPLIES (+12V, ±5V)
- LOW POWER: 462 mW ACTIVE, 20 mW STANDBY (MAX)
- OUTPUT DATA CONTROLLED BY $\overline{CAS}$ AND UNLATCHED AT END OF CYCLE TO ALLOW TWO DIMENSIONAL CHIP SELECTION AND EXTENDED PAGE BOUNDARY
- COMMON I/O CAPABILITY USING "EARLY WRITE" OPERATION
- READ-MODIFY-WRITE, $\overline{RAS}$-ONLY REFRESH, AND PAGE-MODE CAPABILITY
- ALL INPUTS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC CHARGE
- 128 REFRESH CYCLES
- MOSTEK 4116 PIN TO PIN REPLACEMENT
- ECL COMPATIBLE ON V_{BB} POWER SUPPLY (-5.7V)

The M 4116 is a new generation MOS dynamic random access memory circuit organized as 16384 words by 1 bit. The technology used to fabricate the M 4116 is double-poly N-channel silicon gate.
This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry through-out, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin.
Multiplexed address inputs permits the M 4116 to be packaged in a standard 16-pin DIP. The device is available in 16-lead dual in-line ceramic and plastic package.

ABSOLUTE MAXIMUM RATINGS*

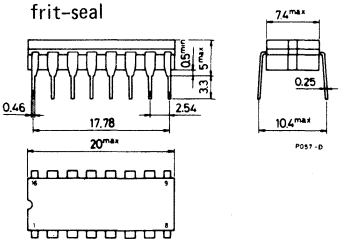
	Voltage on any pin relative to V_{BB}	-0.5 to +20	V
	Voltage on V_{DD}, V_{CC} supplies relative to V_{SS}	-1 to +15	V
	V_{BB}-V_{SS} (V_{DD}-V_{SS} > 0V)	0	V
T_{op}	Operating temperature	0 to +70	°C
T_{stg}	Storage temperature for ceramic package	-65 to +150	°C
	for plastic package	-55 to +125	°C
I_o	Short circuit output current	50	mA
P_{tot}	Total power dissipation	1	W

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

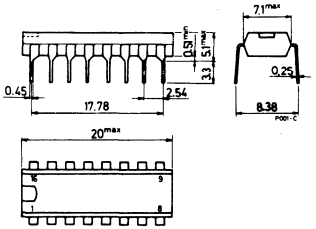
ORDERING NUMBERS: M 4116-2/3/4 B1 for dual in-line plastic package
M 4116-2/3/4 F1 for dual in-line ceramic package, frit-seal

MECHANICAL DATA (dimensions in mm)

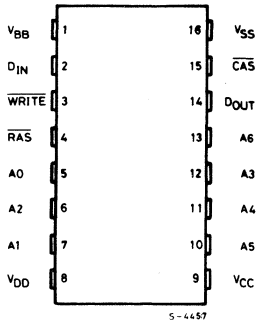
Dual in-line ceramic package
frit-seal



Dual in-line plastic package



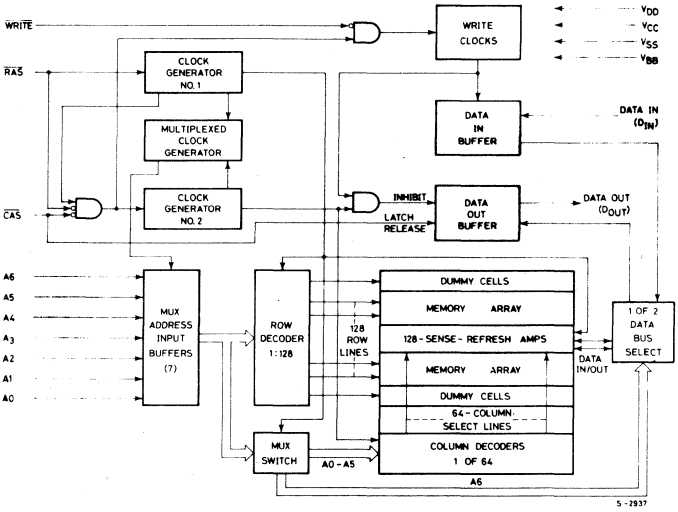
PIN CONNECTIONS



PIN NAMES

A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (-5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+12V)
V_{SS}	GROUND

BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS (T_{amb} = 0 to 70°C)[1]

Parameter		Types			Unit	Note
		Min.	Typ.	Max.		
V_{DD}	Supply voltage	10.8	12	13.2	V	2
V_{CC}	Supply voltage	4.5	5	5.5	V	2.3
V_{SS}	Supply voltage	0	0	0	V	2
V_{BB}	Supply voltage	-4.5	-5	-5.7	V	2
V_{IHC}	Input high voltage on $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	–	7	V	2
V_{IH}	Input high voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	–	7	V	2
V_{IL}	Input low voltage, all inputs	-1	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (T_{amb} = 0 to 70°C)[1], (V_{DD} = 12V±10% V_{CC} = 5V±10%; V_{BB} = -5.7 to -4.5V; V_{SS} = 0V)

Parameter		Test conditions	Types				Unit	Note
			M 4116-2/3		M 4116-4			
			Min.	Max.	Min.	Max.		
I_{DD1}	Average operating current	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{RC}$ (min)		35		35	mA	4
I_{CC1}	Average operating current							5
I_{BB1}	Average operating current			200		200	µA	
I_{DD2}	Standby current	$\overline{RAS} = V_{IHC}$ D_{OUT} = High impedance		1.5		1.5	mA	
I_{CC2}	Standby current		-10	10	-10	10	µA	
I_{BB2}	Standby current			100			µA	
I_{DD3}	Refresh average current	Refresh mode: $\overline{RAS}$ cycling $\overline{CAS} = V_{IHC}$ $t_{RC} = t_{RC}$ (min)		27		27	mA	4
I_{CC3}	Refresh average current		-10	10	-10	10	µA	
I_{BB3}	Refresh average current			200			µA	
I_{DD4}	Page mode average current	Page mode: $\overline{RAS} = V_{IL}$ $\overline{CAS}$ cycling $t_{PC} = t_{PC}$ (min)		27		27	mA	4
I_{CC4}	Page mode average current							5
I_{BB4}	Page mode average current			200			µA	
$I_{I(L)}$	Input leakage current	V_{BB} = -5V 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0 volts	-10	10	-10	10	µA	
$I_{O(L)}$	Output leakage current	D_{OUT} in disabled 0V ≤ V_{OUT} ≤ +5.5V	-10	10	-10	10	µA	
V_{OH}	Output high voltage	I_{OUT} = -5 mA	2.4		2.4		V	3
V_{OL}	Output low voltage	I_{OUT} = 4.2 mA		0.4		0.4	V	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDIT.

(T_{amb} = 0 to 70°C)[1],(V_{DD}=12V±10%; V_{CC}= 5V±10%; V_{SS}=0V, V_{BB}= -5.7 to -4.5V)

Parameter		Types						Unit	Note
		M 4116-2		M 4116-3		M 4116-4			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random read or write cycle time	375		375		410		ns	9
t_{RWC}	Read-write cycle time	375		375		425		ns	9
t_{RMW}	Read modify write cycle time	320		405		500		ns	9
t_{PC}	Page mode cycle time	170		225		275		ns	9
t_{RAC}	Access time from $\overline{RAS}$		150		200		250	ns	10, 12
t_{CAC}	Access time from $\overline{CAS}$		100		135		165	ns	11, 12
t_{OFF}	Output buffer turn-off delay	0	40	0	50	0	60	ns	13
t_T	Transition time (rise and fall)	3	35	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ precharge time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ pulse width	150	10000	200	10000	250	10000	ns	
t_{RSH}	$\overline{RAS}$ hold time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ hold time	150		200		250		ns	
t_{RCD}	$\overline{RAS}$ to CAS delay time	20	50	25	65	35	85	ns	14
t_{CAS}	$\overline{CAS}$ pulse width	100	10000	135	10000	165	10000	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	-20		-20		-20		ns	
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	-10		-10		-10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	50		70		85		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	50		70		85		ns	
t_{DS}	Data-in set-up time	0		0		0		ns	15
t_{DH}	Data-in hold time	45		55		75		ns	15
t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ precharge time (for page mode cycle only)	60		80		100		ns	
t_{REF}	Refresh period		2		2		2	ms	
t_{WCS}	$\overline{WRITE}$ command set-up time	-20		-20		-20		ns	16
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	16
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		175		ns	16

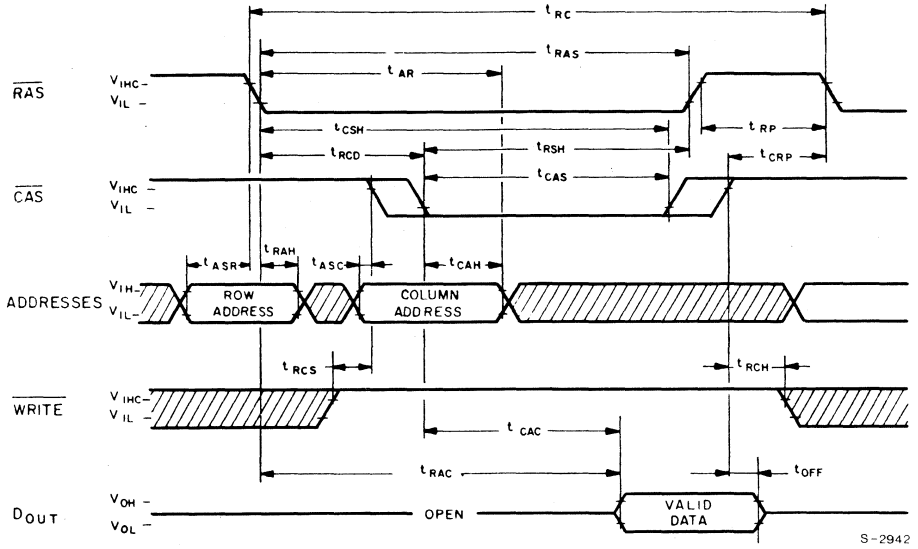
Notes:

1. T_{amb} is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3} and I_{DD4} depend on cycle rate.
5. I_{CC1} and I_{CC4} depend upon output loading. During read out of high level data V_{CC} is connected through a low impedance to data out. At all other times I_{CC} consists of leakage currents only.
6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume $t_T = 5$ ns.
8. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
9. The specifications for t_{RC} (min) and t_{RWC} (min) t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_{amb} \leq 70°C$) is assured.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100 pF.
13. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = \frac{I \Delta t}{\Delta v}$ with $\Delta v = 3$ volts and power supplies at nominal levels.
18. $\overline{CAS} = V_{IHC}$ to disable D_{OUT}.

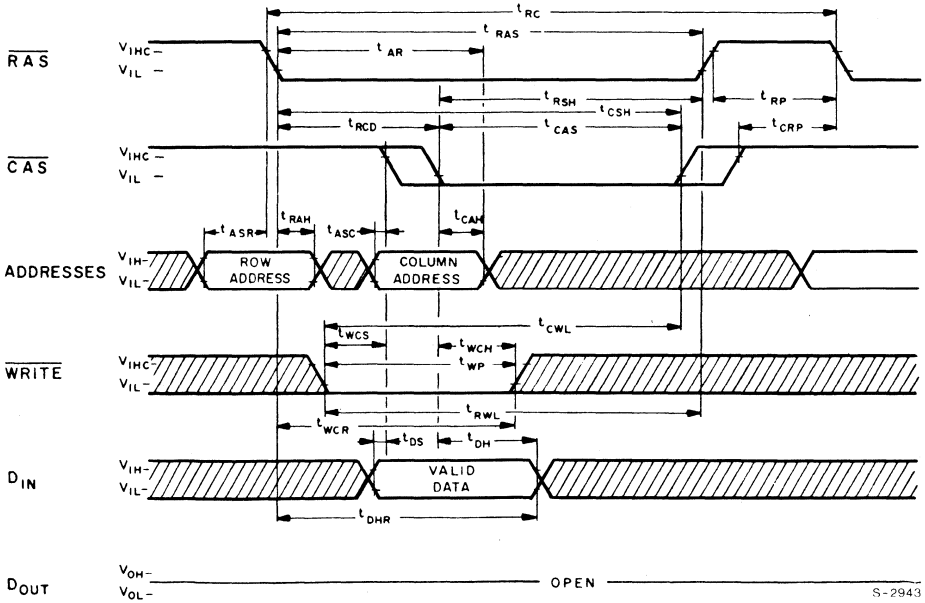
CAPACITANCES (T_{amb} = 0 to 70°C; V_{DD} = 12V ± 10%; V_{SS} = 0V; V_{BB} = -5.7 to -4.5V)

	Parameter	Min.	Typ.	Max.	Unit	Notes
$C_{i\,1}$	Input capacitance (A_0-A_6) DIN		4	5	pF	17
$C_{i\,2}$	Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		8	10	pF	17
C_o	Output capacitance (D_{OUT})		5	7	pF	17, 18

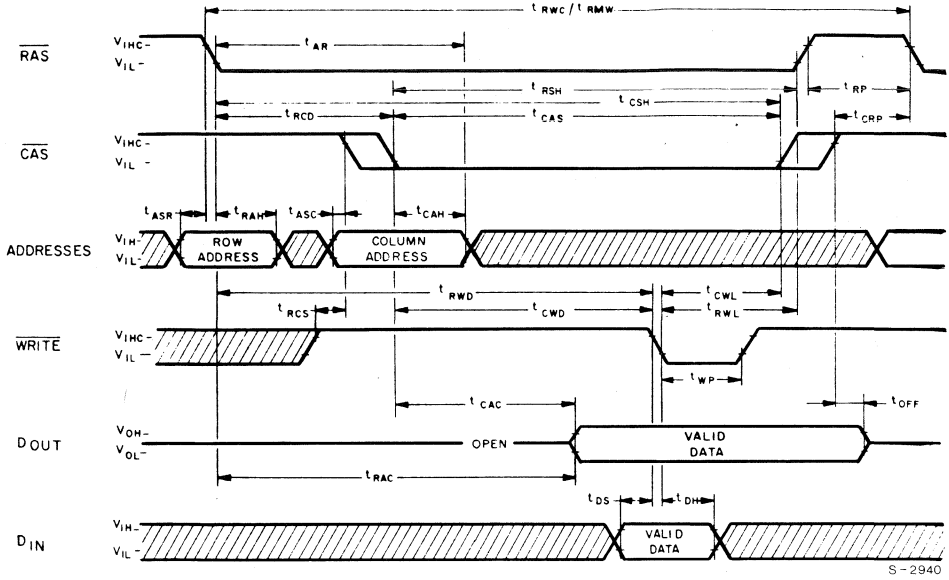
READ CYCLE



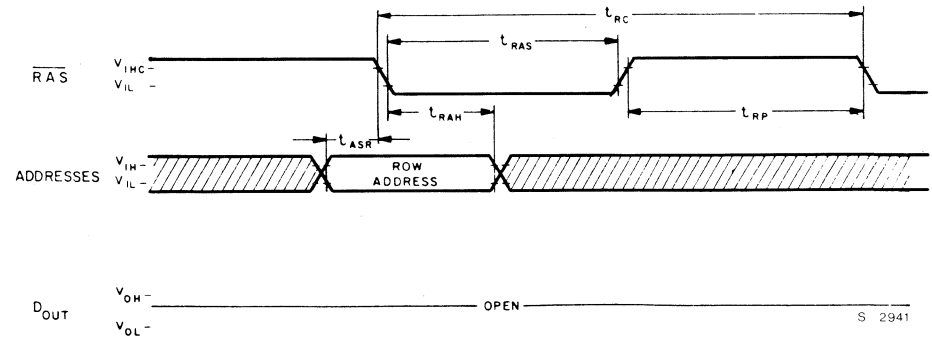
WRITE CYCLE (EARLY WRITE)



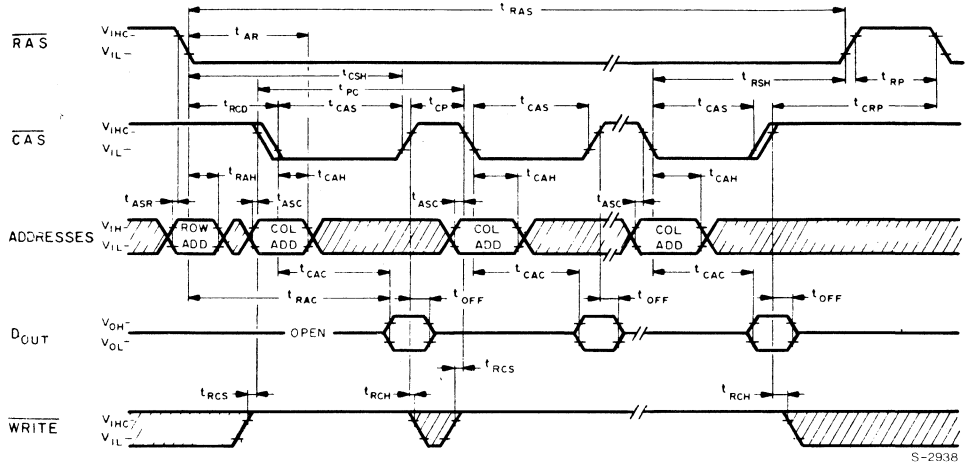
READ-WRITE/READ-MODIFY-WRITE CYCLE



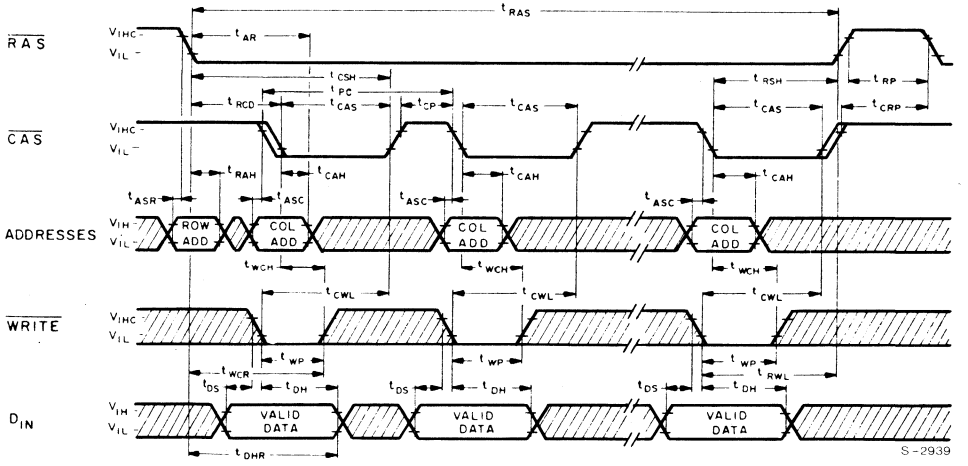
"$\overline{RAS}$-ONLY" REFRESH CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DESCRIPTION

System oriented features include ±10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The M 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the M 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the M 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information. Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end-points result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the M 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the M 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

DATA OUTPUT CONTROL (continued)

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until CAS is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.
If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even through data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).
This type of output operation results in some very significant system implications.

Common I/O Operation – If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.
D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the RAS/CAS clock timing relationship very flexible.
Two Methods of Chip Selection - Since D_{OUT} is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X, Y) chip select array can be realized.
Extended Page Boundary - Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column location in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420Ω maximum and 135Ω typically. The resistance to V_{SS} (logic 0 state) is 95Ω maximum and 35Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the M 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the M 4116 allows for successive memory operations at multiplie column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.
The page boundary of a single M 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and the $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the $I_{DD\,3}$ specification.

POWER CONSIDERATIONS

Most of the circuitry used in the M 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle. This current characteristic of the M4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.
Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the M 4116 draws very little steady state (DC) current.
In system applications requiring lower power dissipations, the operating frequency (cycle rate) of the M 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit equation.

Note: The M4116 is guaranteed to have a maximum I_{DD1} requirement with an ambient temperature range from 0° to 70°C.
1 microsecond cycle, results in a reduced maximum I_{DD1} requirement of under 20 mA with an ambient temperature range from 0 to 70°C.

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the M 4116 overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

POWER UP

The M 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, SGS-ATES recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.
Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).
After power is applied to be device, the M 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

Fig. 1 - I_{DD1} current at minimum cycle time vs. ambient temperature and V_{DD} supply V_{BB} = -4.5V

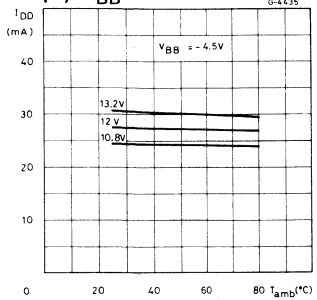


Fig. 2 - I_{DD1} current at minimum cycle time vs. ambient temperature and V_{DD} supply V_{BB} = -5V

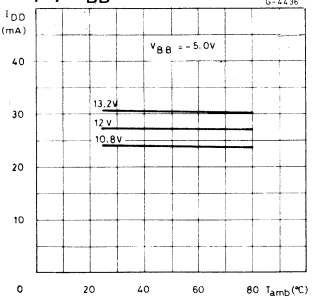


Fig. 3 - I_{DD1} current at minimum cycle time vs. ambient temperature and V_{DD} supply V_{BB} = -5.5V

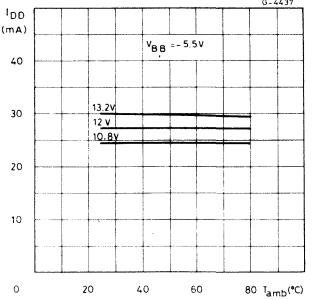


Fig. 4 - Stand by current I_{DD2} at minimum cycle time vs. ambient temperature and V_{DD} supply, V_{BB} = -4.5V

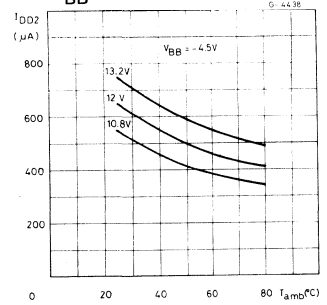


Fig. 5 - Stand by current I_{DD2} at minimum cycle time vs. ambient temperature and V_{DD} supply, V_{BB} = -5V

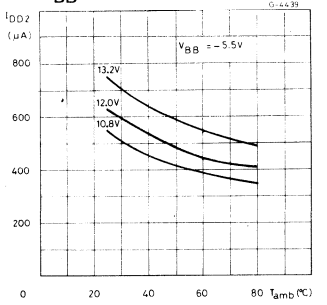


Fig. 6 - Stand by current I_{DD2} at minimum cycle time vs. ambient temperature and V_{DD} supply, V_{BB} = -5.5V

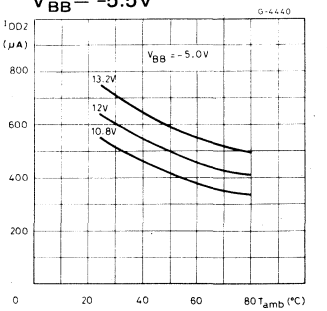


Fig. 7 - Access time from $\overline{RAS}$ vs. ambient temperature and V_{DD} supply, V_{BB} = -4.5V

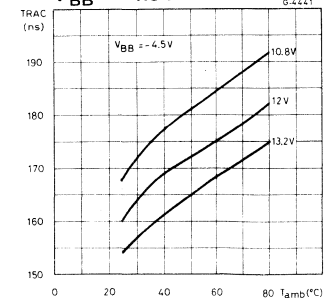


Fig. 8 - Access time from $\overline{RAS}$ vs. ambient temperature and V_{DD} supply, V_{BB} = -5V

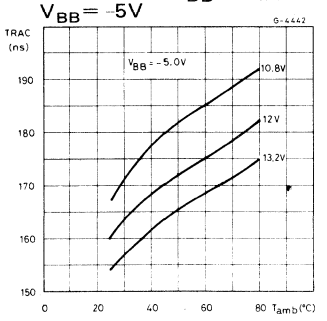


Fig. 9 - Access time from $\overline{RAS}$ vs. ambient temperature and V_{DD} supply, V_{BB} = -5.5V

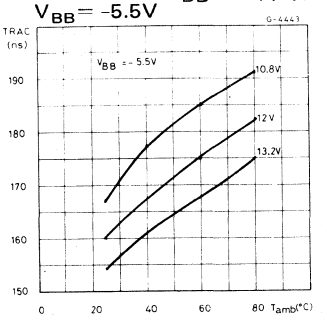


Fig. 10 - Cumulative 2 axis schmoo plot V_{BB} vs. V_{DD}

```
TWO AXIS SHMOO PLOT

                              TEST CONDITIONS

COMNT     BLANK 100%  9 90%  8 80%  7 70%  6 60%  5 50%  4 40%  3 30%  2 20%  1 10%  # 0%
COMNT     PATTERN ADDRESS COMPLEMENT
COMNT     TIMING T3
COMNT     DEVICES TESTED = 49
-------------------------------------------------------------------------------

VBBV   ( V)                                                    TEMP.  =  25  °C

 -7.00
 -6.75
 -6.50
 -6.25
 -6.00
 -5.75
 -5.50
 -5.25
 -5.00
 -4.75
 -4.50
 -4.25
 -4.00
 -3.75
 -3.50
 -3.25
 -3.00.
                    Spec.
        9.00      11.00      13.00      15.00
                             VDDV  ( V)
```

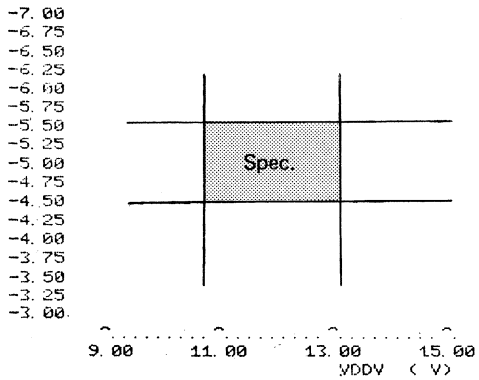


Fig. 11 - 3 axis schmoo plot V_{DD}, V_{BB}, access time

```
THREE AXIS SHMOO PLOT

                              TEST CONDITIONS

COMNT    ****************************************
DEVICE SERIAL NUMBER: 1
COMNT    ****************************************
COMNT      PATTERN ADDRESS COMPLEMENT
COMNT     ALIMENTAZIONI NOMINALI V.  IL = .8V
COMNT      TIMING T4
-------------------------------------------------------------------------------

VBB    ( V)                        TRAC   (NS)                    spec. region

 -7.00 161.0 159.0 157.0 154.0 152.0 150.0 148.0 146.0 145.0 143.0 142.0 141.0 140.0 140.0 139.0 138.0
 -6.75 162.0 160.0 157.0 154.0 152.0 150.0 148.0 146.0 145.0 144.0 142.0 141.0 140.0 140.0 139.0 138.0
 -6.50 162.0 160.0 157.0 154.0 152.0 150.0 148.0 146.0 145.0 144.0 143.0 142.0 141.0 140.0 139.0 138.0
 -6.25 162.0 160.0 157.0 155.0 152.0 150.0 148.0 147.0 145.0 144.0 143.0 142.0 141.0 140.0 139.0 139.0
 -6.00 162.0 160.0 157.0 155.0 152.0 150.0 148.0 147.0 145.0 144.0 143.0 142.0 141.0 140.0 139.0 139.0
 -5.75 162.0 160.0 157.0 155.0 152.0 150.0 148.0 147.0 145.0 144.0 143.0 142.0 141.0 140.0 139.0 139.0
 -5.50 162.0 160.0 158.0 155.0 152.0 150.0 149.0 147.0 145.0 144.0 143.0 142.0 141.0 140.0 139.0 139.0
 -5.25 162.0 160.0 158.0 155.0 153.0 150.0 149.0 147.0 146.0 144.0 143.0 142.0 141.0 140.0 140.0 139.0
 -5.00 162.0 160.0 158.0 155.0 153.0 151.0 149.0 147.0 146.0 144.0 143.0 142.0 141.0 140.0 140.0 139.0
 -4.75 163.0 160.0 158.0 155.0 153.0 151.0 149.0 147.0 146.0 145.0 143.0 142.0 141.0 140.0 140.0 139.0
 -4.50 163.0 160.0 158.0 155.0 153.0 151.0 149.0 147.0 146.0 145.0 144.0 143.0 142.0 141.0 140.0 139.0
 -4.25 163.0 161.0 158.0 156.0 153.0 151.0 149.0 148.0 146.0 145.0 144.0 143.0 142.0 141.0 140.0 139.0
 -4.00 163.0 161.0 158.0 156.0 153.0 151.0 149.0 148.0 146.0 145.0 144.0 143.0 142.0 141.0 140.0 140.0
 -3.75 163.0 161.0 158.0 156.0 153.0 151.0 150.0 148.0 147.0 145.0 144.0 143.0 142.0 141.0 140.0 140.0
 -3.50 164.0 161.0 159.0 156.0 154.0 152.0 150.0 148.0 147.0 145.0 144.0 143.0 142.0 141.0 140.0 140.0
 -3.25 164.0 161.0 159.0 156.0 154.0 152.0 150.0 148.0 147.0 146.0 144.0 143.0 142.0 142.0 141.0 140.0
 -3.00 164.0 162.0 159.0 157.0 154.0 152.0 150.0 149.0 147.0 146.0 145.0 144.0 143.0 142.0 141.0 140.0

        9.20  9.60 10.00 10.40 10.80 11.20 11.60 12.00 12.40 12.80 13.20 13.60 14.00 14.40 14.80 15.20
                                  VDD   ( V)
```

Fig. 12 - Access time distribution for V_{DD}= 12V, V_{BB}= -5V, T_{amb}= 80°C

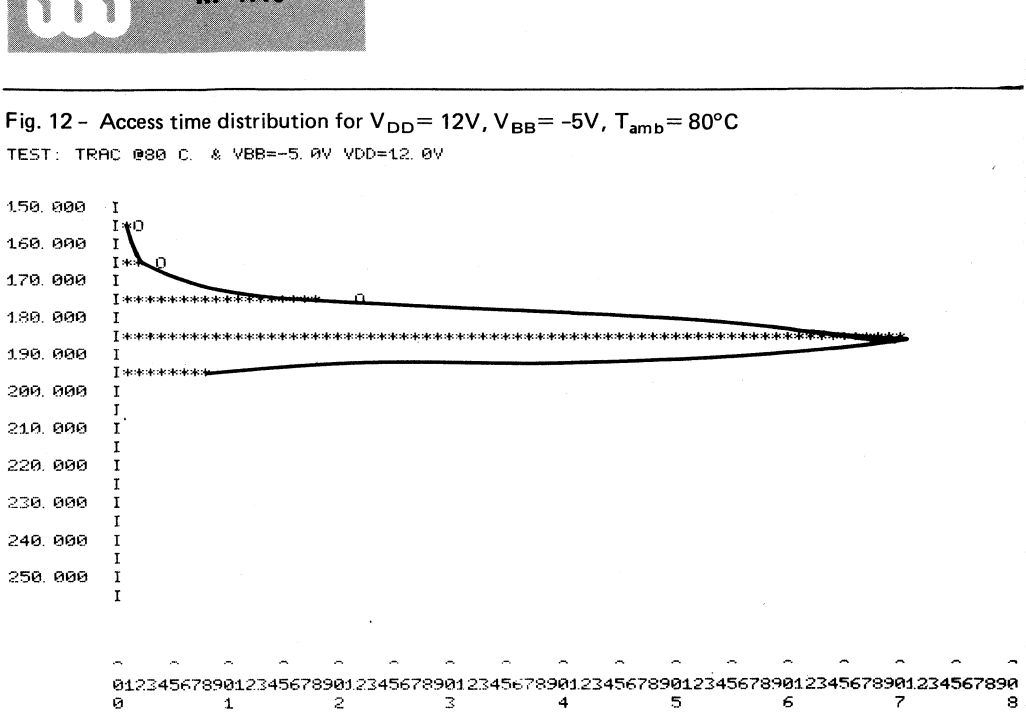


Fig. 13 - Cumulative 2 axis schmoo plot of $V_{IL(max)}$ vs. V_{DD} for addresses (no temperature variation observed)

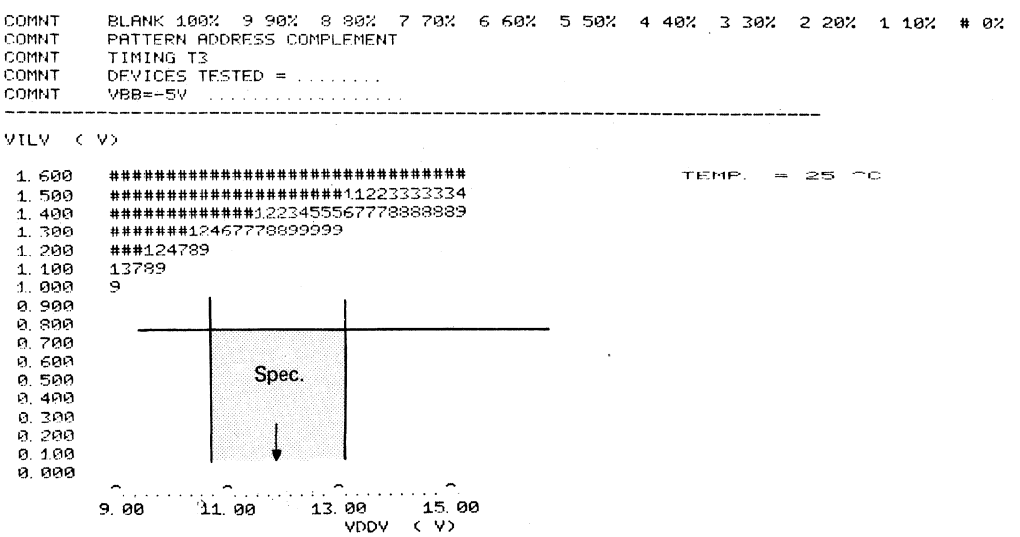
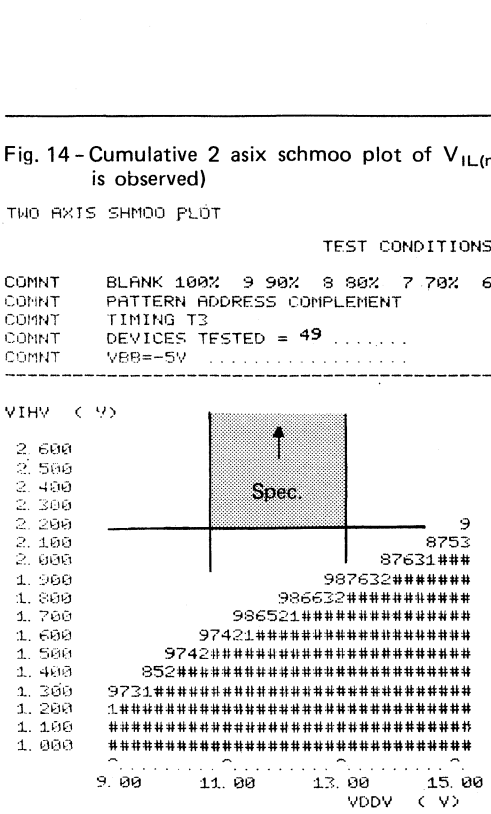


Fig. 14 - Cumulative 2 asix schmoo plot of $V_{IL(max)}$ vs. V_{DD} for addresses (no temperature variation is observed)



COS/MOS INTEGRATED CIRCUIT

M 5156

ADVANCE DATA

A-LAW COMPANDING CODEC

- ±5V POWER SUPPLY
- LOW POWER DISSIPATION -30 mW (TYP.)
- FOLLOWS THE A-LAW COMPANDING CODE
- EXCEEDS CCITT SPECIFICATIONS, INCLUDES EVEN-ORDER-BIT INVERSION
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION
- ON-CHIP SAMPLE AND HOLD
- ON-CHIP OFFSET NULL CIRCUIT ELIMINATES LONG-TERM DRIFT ERRORS AND NEED FOR TRIMMING
- SINGLE 16-PIN PACKAGE
- MINIMAL EXTERNAL CIRCUITRY REQUIRED
- SERIAL DATA OUTPUT OF 64 Kb/s - 2.1 Mb/s at 8 KHz SAMPLING RATE
- SEPARATE ANALOG AND DIGITAL GROUNDING PINS REDUCE SYSTEM NOISE PROBLEMS

The M5156 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the A-law companding code and (2) a digital-to-analog converter which also conforms to the A-law code.
These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in PCM systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64 Kb/s - 2.1 Mb/s rate with analog signal sampling occurring at an 8 KHz rate. A sync pulse input is provided for synchronizing transmission and reception of multichannel information being multiplexed over a single transmission line.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+	+6	V
DC Supply Voltage, V-	-6	V
Operating Temperature range	0 to 70	°C
Storage Temperature range	-55 to +125	°C
Package Dissipation at 25°C (Derated 9 mW/°C when soldered into PCB)	500	mW
Digital Input	$-0.5 \leqslant V_{IN} \leqslant V+$	V
Analog Input	$V- \leqslant V_{IN} \leqslant V+$	V
$+V_{REF}$	$-0.5 \leqslant +V_{REF} \leqslant V+$	V
$-V_{REF}$	$V- \leqslant -V_{REF} \leqslant +0.5$	V

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

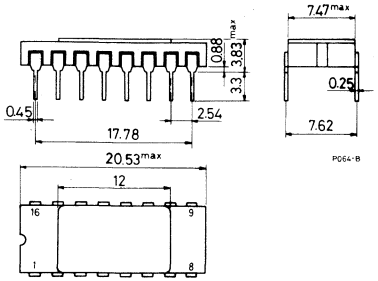
ORDERING NUMBERS:

M5156 D1 for dual in-line ceramic package, metal-seal
M5156 F1 for dual in-line ceramic package, frit-seal

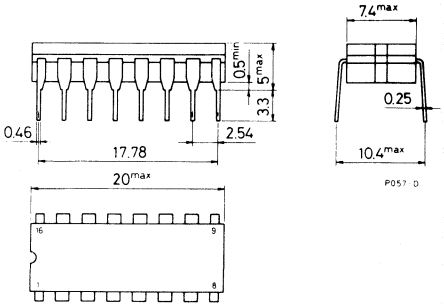
M 5156

MECHANICAL DATA (dimensions in mm)

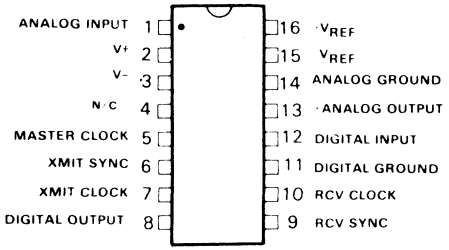
Dual in-line ceramic package, metal-seal



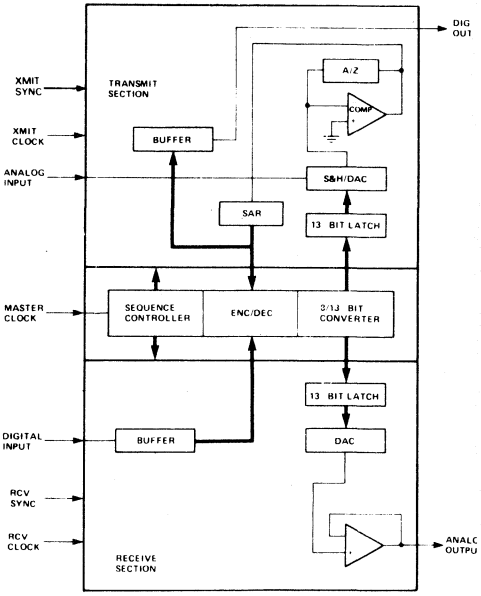
Dual in-line ceramic package, frit-seal



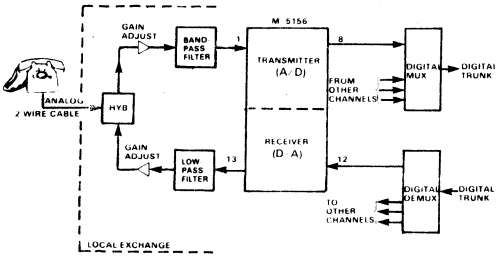
PIN CONNECTIONS



BLOCK DIAGRAM



PCM SYSTEM



POWER SUPPLY REQUIREMENTS

Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V-	Negative Supply Voltage	-5.25	-5.0	-4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	-2.625	-2.5	-2.375	V	1

DC CHARACTERISTICS (Test conditions: V+= 5.0V, V-= -5.0V, $+V_{REF}$= 2.5V, $-V_{REF}$= -2.5V)

Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	
$V_{OFFSET/I}$	Analog Input Offset Voltage		± 1	± 8	mV	
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$(V_{OFFSET/O})$	Analog Output Offset Voltage		-200	±850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN}= 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	± 10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN}= 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	± 10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	
I−	Negative Supply Current		2	6	mA	
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 3 and Figure 4)

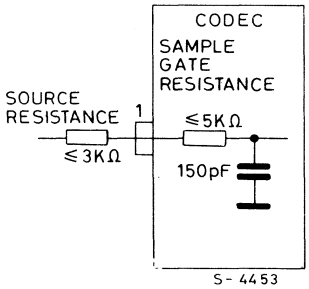
Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
F_M	Master Clock Frequency	1.5	2.048	2.1	MHz	
F_R, F_X	XMIT, RCV. Clock Frequency	0.064	2.048	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{CLK}	ns	
t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of $t_{FC}(t_{RS})$			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay		200		ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50		ns	4
t_{DOR}	Digital Output Rise Time		50		ns	4
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of $t_{RC}(t_{FS})$			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	5
t_{RDH}	RCV. Data Hold Time	200			ns	5
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	5
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
SLEW+	Analog Output Positive Slew Rate		1		$V/\mu s$	
SLEW-	Analog Output Negative Slew Rate		1		$V/\mu s$	
DROOP	Analog Output Droop Rate		25		$\mu V/\mu s$	

SYSTEM CHARACTERISTICS (Refer to Figures 10 and 11)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
S/D	Signal-to-Distortion Ratio	Analog Input = 0 to -30 dBmO Analog Input = -40 dBmO Analog Input = -45 dmO	35 29 24	39 34 29		dB dB dB
GT	Gain Tracking	Analog Input = +3 to -37 dBmO Analog Input = -37 to -50 dBmO Analog Input = -50 to -55 dBmO	-0.4 -0.8 -2.5	± 0.1 ± 0.1 ± 0.2	+0.4 +0.8 +2.5	dB dB dB
N_{IC}	Idle Channel Noise	Analog Input = 0 Volts		-80	--72	dBmOp
TLP	Transmission Level Point	600 Ω		+4		dB

Notes:
1. $+V_{REF}$ and $-V_{REF}$ must be matched with in ±1% in order to meet system requirements.
2. Sampling is accomplished by changing the internal capacitor to within ½ LSB (≤ 300 μV) in 20 μs. Therefore, the external source resistance must be 3k or less. The equivalent circuit during sampling is shown on the right.
3. The M5156 will I source current through an internal 6 kΩ resistor to help pull up the TTL output. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30 pF with I_{OH}= -100 μA, I_{OL}= 500 μA.
5. The first bit of data is loaded when Sync. and Clock are both "1" during bit time 1 as shown on RCV, timing diagram.
6. This delay is necessary to avoid overlapping Clock and Sync.

EQUIVALENT INPUT RESISTANCE CIRCUIT DURING SAMPLING



FUNCTIONAL DESCRIPTION

Pin 1 — Analog Input

Voice-frequency analog signals which are bandwidth-limited to 4 kHz are input at this pin. Typically, they are then sampled at an 8 kHz rate (Refer to Figure 1). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion.

Pin 5 — Master Clock

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV, CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

FUNCTIONAL DESCRIPTION (continued)

Fig. 1 - A/D, D/A conversion timing

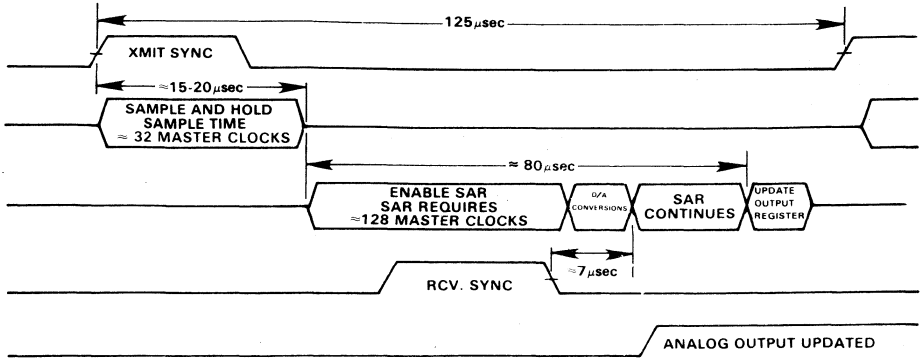
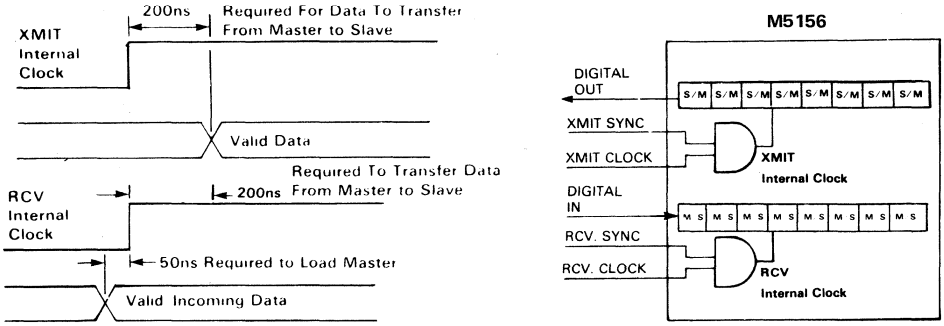


Fig. 2 - Data input/output timing

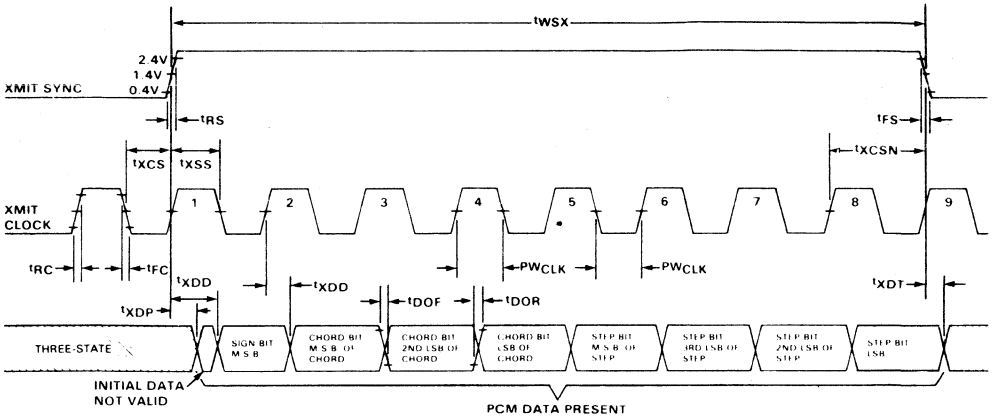


Pin 6 — XMIT SYNC (Refer to Figure 3 for the Timing Diagram)
This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word (Refer to Figure 7).

Pin 7 — XMIT CLOCK (Refer to Figure 3 for the Timing Diagram)
The on-chip 8-bit output shift register of the M5156 is unloaded at the clock rate present on this pin. Clock rates of 64 kHz - 2.1 MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 2). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

FUNCTIONAL DESCRIPTION (continued)

Fig. 3 - Transmitter section timing



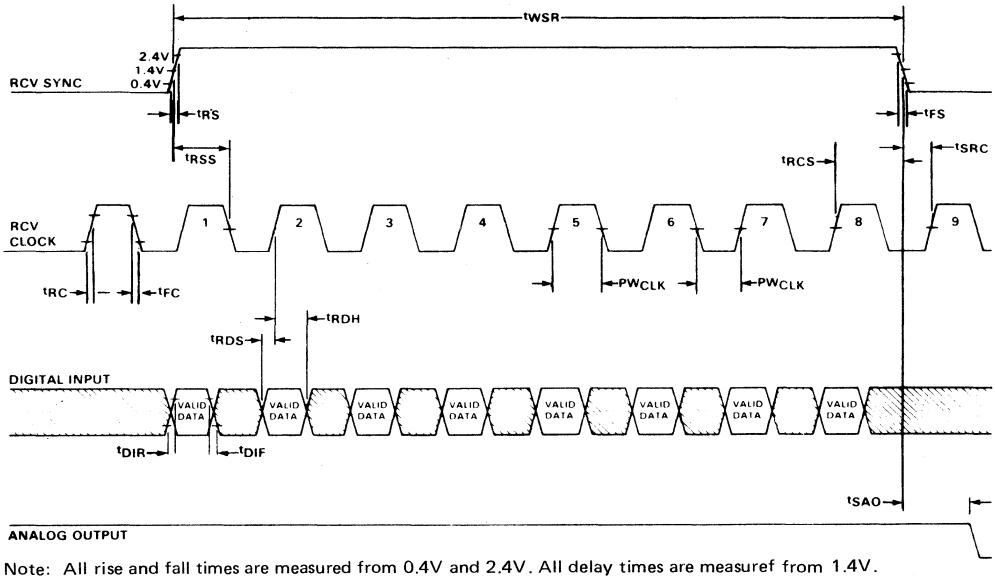
Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Pin 9 — RCV. SYNC (Refer to Figure 4 for the Timing Diagram)
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV. SYNC. pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 1). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 8).

Pin 10 — RCV. CLOCK (Refer to Figure 4 for the Timing Diagram)
The on-chip 8-bit shift register for the M5156 is loaded at the clock rate present on this pin. Clock rates of 64 kHz - 2.1 MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 2). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

FUNCTIONAL DESCRIPTION (continued)

Fig. 4 - Receiver section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measuref from 1.4V.

Fig. 5 - A/D converter (A-Law Encoder) transfer characteristic

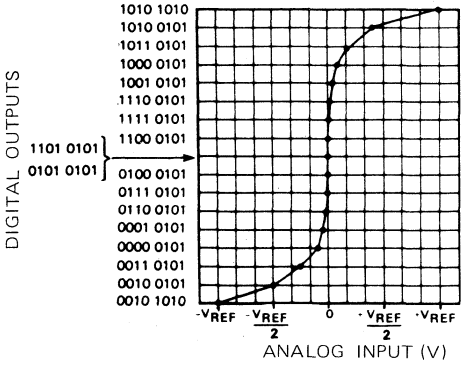
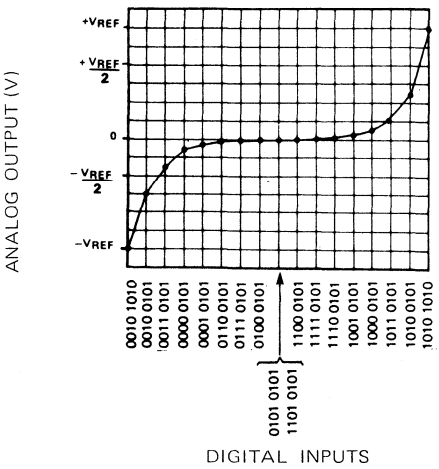


Fig. 6 - D/A converter (A-Law Decoder) transfer characteristic



FUNCTIONAL DESCRIPTION (continued)

Table 1 - Digital output code: A Law

Chord Code	Chord Value	Step Value
1. 101	0.0 mV	1.221 mV
2. 100	20.1 mV	1.221 mV
3. 111	40.3 mV	2.44 mV
4. 110	80.6 mV	4.88 mV
5. 001	161.1 mV	9.77 mV
6. 000	332 mV	19.53 mV
7. 011	645 mV	39.1 mV
8. 010	1.289 V	78.1 mV

EXAMPLE:

1 110 0111=+80.6mV+(2x4.88mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

Pin 8 — Digital Output

The M5156 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first two Chords, the Step Bit has a value of 1.2 mV. In the third Chord, the Step Bit has a value of 2.4 mV. This doubling of the step value continues for each of the five successive Chords. Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (**Refer to Table 1**). Thus the output, which follows the A-law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (A-law Encoder) is shown in Figure 5.

Pin 12 — Digital Input

The M5156 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 4. When RCV. SYNC goes high, the M5156 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (A-law Decoder) is shown in Figure 6.

Pin 13 — Analog Output

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

Pins 16 and 15 — Positive and negative reference voltages ($+V_{REF}$ and $-V_{REF}$)

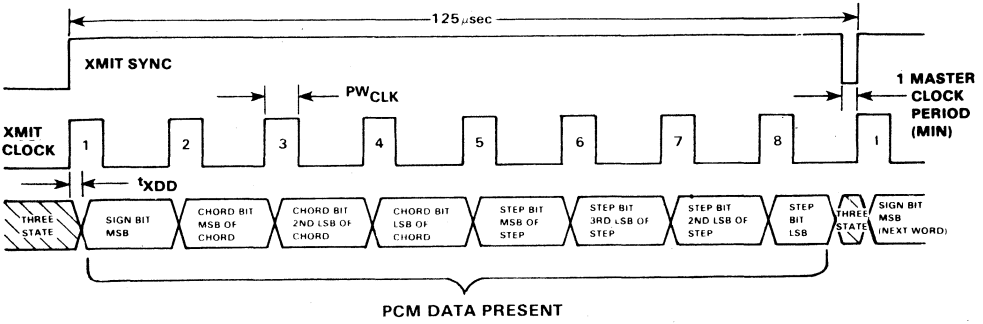
These inputs provide the conversion references for the digital-to-analog converters in the M5156. $+V_{REF}$ and $-V_{REF}$ must maintain 100 ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

OPERATION OF DECODEC WITH 64 kHz XMIT/RCV.

Clock Frequencies

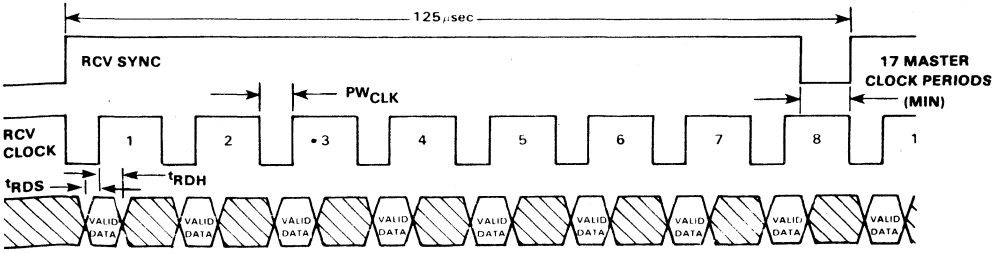
XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figs. 7 and 8).

Fig. 7 - 64 kHz operation, transmitter section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Fig. 8 - 64 kHz operation, receiver section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Offset Null

The offset null feature of the M5156 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

Performance Evaluation

The equipment connections shown in Figure 9 can be used to evaluate the performance of the M5156. An analog signal provided by the HP3552A Transmission Test Set is connected to the Analog Input (Pin 1) of the M5156. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3552A. Remaining pins of the M5156 are connected as follows:

(1) RCV. SYNC is tied to XMIT SYNC.
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

(1) MASTER CLOCK = 2.048 MHz.
(2) XMIT SYNC repetition rate = 8 kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods.

When all the above requirements are met, the setup of Figure 9 permits the measurement of synchronous system performance over a wide range of analog inputs.
The data register and ideal decoder provide a means of checking the encoder portion of the M5156 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also. Some experimental results obtained with the M5156 are shown in Figs. 10 and 11.

Fig. 9 - System characteristics test configuration

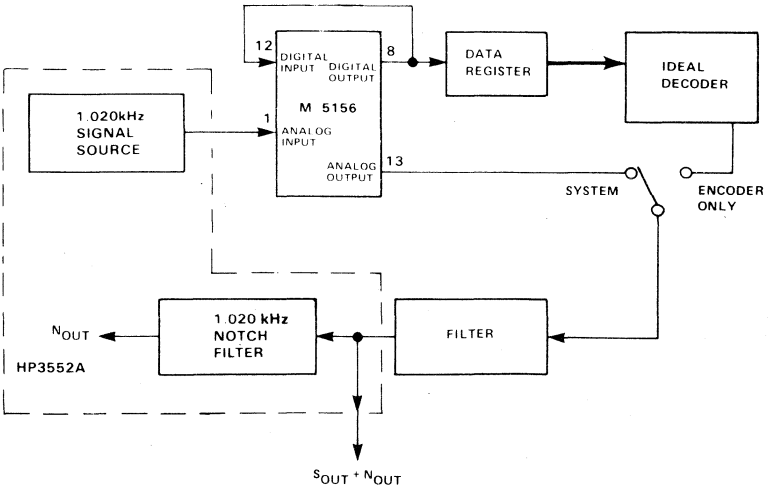


Fig. 10 - S/D ratio vs. input level

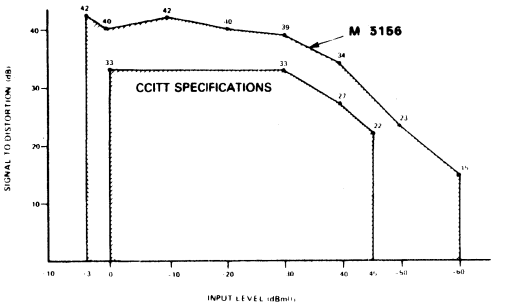
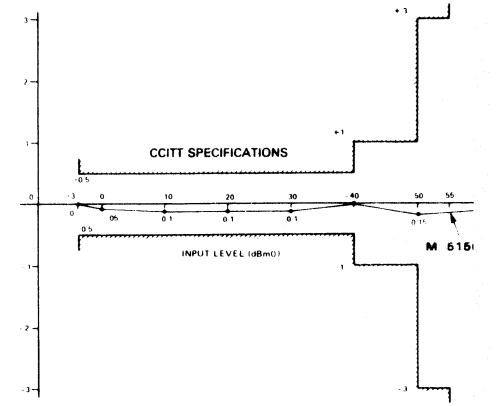


Fig. 11 - Gain tracking performance



MOS INTEGRATED CIRCUIT

M 5912

ADVANCE DATA

PCM TRANSMIT/RECEIVE FILTERS

- MONOLITHIC DEVICE INCLUDES BOTH TRANSMIT AND RECEIVE FILTERS
- CCITT G712 AND AT&T D3/D4 COMPATIBLE
- TRANSMIT FILTER INCLUDES 50/60 Hz REJECTION
- RECEIVE FILTER INCLUDES SIN X/X COMPENSATION
- EXTERNAL GAIN ADJUSTMENT, BOTH TRANSMIT AND RECEIVE FILTERS
- LOW POWER CONSUMPTION: 20 mW TYPICAL WITHOUT POWER AMPLIFIERS
  < 1 mW TYPICAL IN POWER-DOWN MODE
- DIRECT INTERFACE WITH TRANSFORMER OR ELECTRONIC TELEPHONE HYBRIDS
- ± 5% POWER SUPPLIES; +5V, -5V
- STANDARD 16-PIN PACKAGE
- PIN-FOR-PIN COMPATIBLE WITH THE 2912 PCM FILTER

The M5912 is a monolithic device containing the two filters of a PCM line or trunk termination and is designed to minimize power dissipation, maximize reliability and provide a low-cost alternative to hybrid filters. The device consists of two switched-capacitor filters, transmit and receive, and power amplifiers which may be used to drive a transformer hybrid (2-to-4 wire converter) or an electronic hybrid (SLIC). If an electronic hybrid is used, the power amplifiers are not needed and may be deactivated to minimize power dissipation. The transmit filter is a band-pass filter which will pass frequencies between 300 Hz and 3200 Hz and provides rejection of the 50/60 Hz power line frequency as well as the anti-aliasing needed in an 8 kHz sampling system. The receive filter is a low-pass filter which smooths the voltage steps present in the CODEC output waveform and provides the sin x/x correction necessary to give unity gain in the passband for the CODEC-decoder-and-receive-filter pair.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage with Respect to V_{BB}	-0.3 to +14.0	V
All Input and Output Voltages with Respect to V_{BB}	-0.3 to +14.0	V
All Output Currents	± 50	mA
Temperature Under Bias	-10 to +80	°C
Storage Temperature range	-65 to +150	°C
Package Dissipation at 25°C (Derated 9 mW/°C when soldered into PCB)	500	mW

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

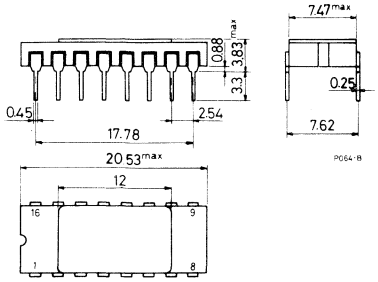
ORDERING NUMBERS:

M5912 D1 for dual in-line ceramic package, metal seal
M5912 F1 for dual in-line ceramic package, frit seal

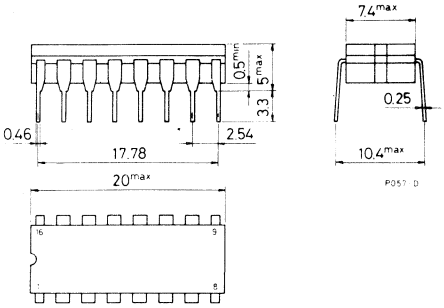
M 5912

MECHANICAL DATA (dimensions in mm)

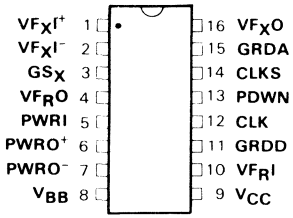
Dual in-line ceramic package metal-seal



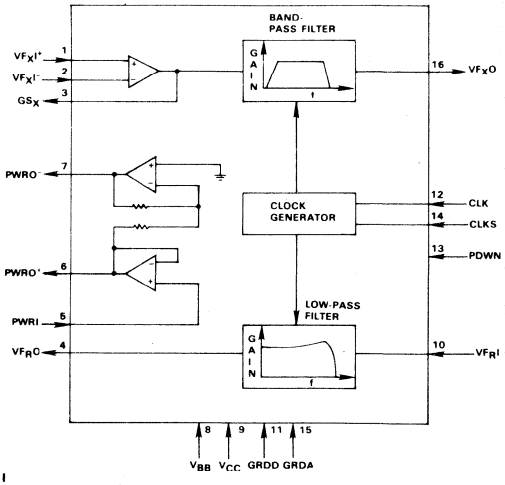
Dual in-line ceramic package frit-seal



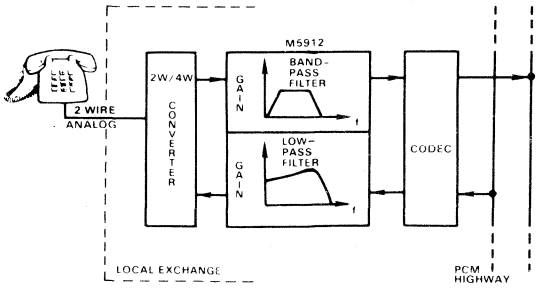
PIN CONNECTIONS



BLOCK DIAGRAM



TYPICAL LINE TERMINATION



POWER DISSIPATION

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{CC0}	V_{CC} Standby Current	PDWN = V_{IH} min			100	µA
I_{BB0}	V_{BB} Standby Current	PDWN = V_{IH} min			100	µA
I_{CC1}	V_{CC} Operating Current, Power Amplifiers Inactive	PWRI = V_{BB}			6	mA
I_{BB1}	V_{BB} Operating Current, Power Amplifiers Inactive	PWRI = V_{BB}			6	mA
I_{SCPA}	Short Circuit Output Current (Power Amplifier)	Either power amplifier to ground			20	mA

DC AND OPERATING CHARACTERISTICS (T_{amb}= 0°C to +70°C, V_{CC}= +5V ± 5%, V_{BB}= -5V ± 5%, GRDA= 0V, GRDD = 0V, unless otherwise specified)

DIGITAL INTERFACE

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LIC}	Input Load Current	V_{IN} = V_{IL} min to V_{IH} max			10	µA
I_{LIO}	Input Load Current, CLKS	V_{IN} = V_{BB} to V_{IH} max			50	µA
I_{LIP}	Input Load Current, PDWN	V_{IN} = V_{IL} min to V_{IH} max			-40	µA
V_{IL}	Input Low Voltage (except CLKS)				0.8	V
V_{IH}	Input High Voltage (except CLKS)		2.2			V
V_{ILO}	Input Low Voltage, CLKS		V_{BB}		V_{BB}+0.5	V
V_{IIO}	Input Intermediate Voltage, CLKS		GRDD-0.5		0.2	V
V_{IHO}	Input High Voltage, CLKS		V_{CC}-0.5		V_{CC}	V

ANALOG INTERFACE, TRANSMIT FILTER GAIN SETTING AMPLIFIER

I_{BXI}	Input Leakage Current, VF_XI^+, VF_XI^-	-3.2V < V_{IN} < 3.2V			100	nA
R_{IXI}	Input Resistance, VF_XI^- VF_XI^+		10			MΩ
V_{OSXI}	Input Offset Voltage, VF_XI^+, VF_XI^-	-3.2V < V_{IN} < 3.2V			25	mV
$PSRR_1$	Power Supply Rejection, GS_X		60			dB

DC AND OPERATING CHARACTERISTICS (continued)

ANALOG INTERFACE, TRANSMIT FILTER GAIN SETTING AMPLIFIER

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
CMRR	Common Mode Rejection, VF_XI^+, VF_XI^-	$-3.2V < V_{IN} < 3.2V$	60			dB
A_{VOL}	DC Open Loop Voltage Gain, GS_X		2000			
f_C	Open Loop Unity Gain Bandwidth, GS_X			2		MHz
V_{OXI}	Output Voltage Swing, GS_X	$R_L \geq 10\ k\Omega$	± 2.5			V
C_{LXI}	Load Capacitance, GS_X				20	pF
R_{LXI}	Minimum Load Resistance, GS_X	Minimum R_L	10			kΩ

ANALOG INTERFACE, TRANSMIT FILTER

R_{OX}	Output Resistance, VF_XO				100	Ω
V_{OSX}	Output DC Offset, VF_XO	VF_XI^+ Connected to GRDA, Input Op amp at Unity Gain			200	mV
$PSRR_2$	Power Supply Rejection of V_{CC} at 1 kHz, VF_XO		35	40		dB
$PSRR_3$	Power Supply Rejection of V_{BB} at 1 kHz, VF_XO		25	30		dB
C_{LX}	Load Capacitance, VF_XO				20	pF
R_{LX}	Minimum Load Resistance, VF_XO	Minimum R_L	3			kΩ
V_{OX}	Output Voltage Swing, 1 kHz, VF_XO	$R_L \geq 10\ k\Omega$		± 3.2		V
		$R_L \geq 3\ k\Omega$	± 2.5			

ANALOG INTERFACE, RECEIVE FILTER

I_{BR}	Input Leakage Current, VF_RI	$-3.2V < V_{IN} < 3.2V$			1	μA
RIR	Input Resistance, VF_RI		2			MΩ
R_{OR}	Output Resistance, VF_RO				100	Ω
V_{OSR}	Output DC Offset, VF_RO	VF_RI Connected to GRDA			200	mV
$PSRR_4$	Power Supply Rejection of V_{CC} at 1 kHz, VF_RO		30	35		dB
$PSRR_5$	Power Supply Rejection of V_{BB} at 1 kHz, VF_RO		30	35		dB
C_{LR}	Load Capacitance, VF_RO				20	pF
R_{LR}	Minimum Load Resistance, VF_RO	Minimum R_L	10			kΩ
V_{OR}	Output Voltage Swing, VF_RO	$R_L = 10\ k\Omega$	± 3.2			V

DC AND OPERATION CHARACTERISTICS (continued)

ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{BRA}	Input Leakage Current, PWRI	$-3.2C < V_{IN} < 3.2V$			3	μA
R_{IRA}	Input Resistance, PWRI		10			MΩ
R_{ORA}	Output Resistance, PWRO+, PWRO−	$\|I_{OUT}\| < 10$ mA $-3.2V < V_{OUT} < 3.2V$			1	Ω
V_{OSRA}	Output DC offset, PWRO+, PWRO−	PWRI Connected to GRDA			50	mV
C_{LRA}	Lead Capacitance, PWRO+, PWRO−				100	pF
V_{ORA1}	Output Voltages Swing Across R_L, PWRO+, PWRO− Single Ended Connection	$R_L \geq 300\Omega$ R_L Connected to GRDA	± 3.2			V
V_{ORA2}	Output Voltage Swing, PWRO+, PWRO− Balanced Output Connection	$R_L \geq 600\Omega$ R_L Connected between PWRO+ and PWRO−	± 6.4			V

AC CHARACTERISTICS (T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA = 0V, GRDD = 0V, unless otherwise specified).

Clock Input Frequency: CLK = 1.536 MHz ± 0.1%, CLKS = V_{ILO} (Tied to V_{BB})
CLK = 1.544 MHz ± 0.1%, CLKS = V_{IIO} (Tied to GRDD)
CLK = 2.048 MHz ± 0.1%, CLKS = V_{IHO} (Tied to V_{CC})
CLK = 2.560 MHz ± 0.1%, CLKS = Open Circuit

TRANSMIT FILTER TRANSFER CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
G_{RX}	Gain Relative to Gain at 1 kHz	OdBmO Input Signal Gain Setting Op Amp at Unit Gain				
	Below 50 Hz					dB
	50 Hz				-35	dB
	60 Hz		-26		-30	dB
	200 Hz	OdBmO Signal = 1.2 V_{RMS}, Input at VF_XI^-	-1.8		-0.125	dB
	300 Hz to 3000 Hz		-0.125		+0.125	dB
	3300 Hz		-0.65		0.03	dB
	3400 Hz	Output at VF_XO is ≈ 1.73 V_{RMS}	-1.4		-0.1	dB
	4000 Hz				-14.5	dB
	4600 Hz and Above				-33	dB

AC CHARACTERISTICS (continued)

TRANSMIT FILTER TRANSFER CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
G_{AX}	Absolute Passband Gain at 1 kHz, VF_XO		2.9	3.0	3.1	dB
G_{AXT}	Gain Variation with Temperature at 1 kHz	OdBmO Signal Level		0.0005		dB/°C
G_{AXS}	Gain Variation with Supplies at 1 kHz	OdBmO Signal Level, Supplies ± 5%		0.05		dB/V
CT_{RT}	Cross Talk, Receive to Transmit, Measured at VF_XO	VF_RI = 1.2 V_{RMS}, 1 kHz Input VF_XI^+, VF_XI^- Connected to GS_X, GS_X Connected through 10 kΩ to GRDA			-60	dB
N_{CX1}	Total C Message Noise at Output, VF_XO	Gain Setting Op Amp at Unity Gain		6		dBrncO
N_{CX2}	Total C Message Noise at Output, VF_XO	Gain Setting Op Amp at 20 dB Gain		10		dBrncO
D_{DX}	Differential Envelope Delay, VF_XO 1 kHz to 2.6 kHz				40	μs
D_{AX}	Absolute Delay at 1 kHz, VF_XO				195	μs
DP_{X1}	Single Frequency Distortion Products	OdBm Input Signal at 1 kHz			-50	dB
DP_{X2}	Single Frequency Distortion Products at Maximum Signal Level of +3 dBmO at VF_XO	Gain Setting Op Amp at 20 dB Gain. The +3 dBmO signal at VF_XO is 1.73 V_{RMS}			-45	dB

AC CHARACTERISTICS (T_{amb} = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, GRDA= 0V, GRDD= 0V, unless otherwise specified).

Clock Input Frequency: CLK = 1.536 MHz ± 0.1%, CLKS = V_{ILO} (Tied to V_{BB})
CLK = 1.544 MHz ± 0.1%, CLKS = V_{IIO} (Tied to GRDD)
CLK = 2.048 MHz ± 0.1%, CLKS = V_{IHO} (Tied to V_{CC})
CLK = 2.560 MHz ± 0.1%, CLKS = Open Circuit

RECEIVE FILTER TRANSFER CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
G_{RR}	Gain Relative to Gain at 1 kHz with sinx/x Correction	OdBmO Input Signal				
	Below 200 Hz	OdBmO Signal ≅ 1.2 V_{RMS}X			0.125	dB
	200 Hz		-0.125		0.125	dB
	300 Hz to 3000 Hz	$\left(\text{Sin}\frac{\pi f}{(8000)} / \frac{\pi f}{(8000)}\right)$,	-0.125		0.125	dB
	3300 Hz	Input at VF_RI	-0.65		0.03	dB
	3400 Hz		-1.4		-0.1	dB

AC CHARACTERISTICS (continued)

RECEIVE FILTER TRANSFER CHARACTERISTICS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
G_{RR}	4000 Hz				-14.5	dB
	4600 Hz and Above				-32	dB
G_{AR}	Absolute Passband Gain at 1 kHz, VF_RO		-0.1	0	+0.1	dB
G_{ART}	Gain Variation with Temperature at 1 kHz	0dBmO Signal Level		0.0005		dB/°C
G_{ARS}	Gain Variation with Supplies at 1 kHz	0dBmO Signal Level, Supplies ± 5%		0.05		dB/V
CT_{TR}	Cross Talk, Transmit to Receive, Measured at VF_RO	VF_XO = 1.73 V_{RMS}, 1 kHz Output. VF_RI Connected to GRDA			-60	dB
N_{CR}	Total C Message Noise at Output, VF_RO	VF_RO Output or $PWRO^+$ and $PWRO^-$ Connected with Unity Gain		6		dBrnc0
D_{DR}	Differential Envelope Delay, VF_RO, 1 kHz to 2.6 kHz				120	µs
D_{AR}	Absolute Delay at 1 kHz, VF_RO				125	µs
DP_{R1}	Single Frequency Distortion Products	0dBm Input Signal at 1 kHz			-50	dB
DP_{R2}	Single Frequency Distortion Products at Maximum Signal Level of +3 dBmO at VF_RO	+3 dBmO Signal Level of 1.73 V_{RMS}, 1 kHz Input at VF_RO			-45	dB

FUNCTIONAL DESCRIPTION

Pin 1 – VF_XI^+

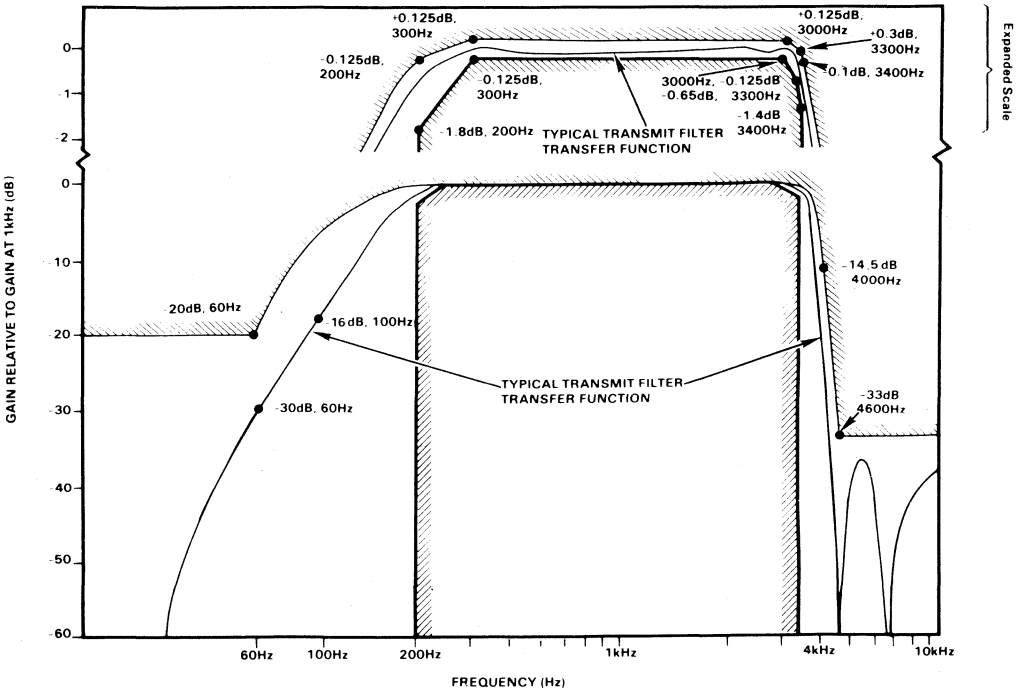
Pin 1 is the non-inverting input of the gain adjustment op amp in the transmit filter seciton. The signal applied to this pin typically comes from the transmit leg of a 2-to-4 wire hybrid. This input may be AC or DC coupled. This signal passes through the op amp to the transmit (band-pass) switched-capacitor filter which will pass frequencies between 300 and 3200 Hz, provide rejection of the 50/60 Hz power line frequency and provide antialiasing for an 8 kHz sampling system. This filter exceeds AT&T D3 and D4 specifications and is compatible with the CCITT G712 recommendations. Its specifications meet the digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications are shown in Figure 1.

Pin 2 – VF_XI^-

Pin 2 is the inverting input of the gain adjustment op amp on the transmit filter. A return path for the op-amp output is provided by GS_X, Pin 3. Pins 2 and 3 may be used to provide gain up to 20 dB without degrading the noise performance of the filters.
This op amp has a common mode range of ± 2.5V, low DC offset (2.5 mV typ.) and can provide a voltage gain greater than 2000. The unity gain bandwidth is approximately 2 MHz. The transmit filter, excluding the input op amp, provides a gain of +3 dB in the passband.

FUNCTIONAL DESCRIPTION (continued)

Fig. 1 - Transmit filter transfer characteristics



Pin 3 – GS_X

Pin 3 is connected to the output of the gain-adjustment op amp in the transmit filter section. For proper operation, the load impedance connected to the GS_X output should be greater than 10 KΩ in parallel with 20 pF (Refer to Figure 2).

Pin 4 – VF_RO

Pin 4 is the output of the receive (low-pass) filter and is capable of driving high impedance electronic hybrids. The gain of the receive signal may be attenuated by using a resistor divider as shown in Figure 2. The resistive load connected to VF_RO should be greater than 10 KΩ.
If the receive filter is to drive a transformer hybrid, VF_RO should be connected to PWRI (Pin 5) as shown in Figure 3.

Pin 5 – PWRI

Pin 5 provides the input to the power driver amplifiers which interface the receive filter to a transformer hybrid. PWRI is a high impedance input which can be driven by VF_RO directly. The input voltage range is ± 3.2V and the gain for a bridged output is 6 dB. The power amplifiers may be deactivated when not being utilized by tying PWRI to V_{BB}.

FUNCTIONAL DESCRIPTION (continued)

Fig. 2 - Transmit and receive gain adjustment

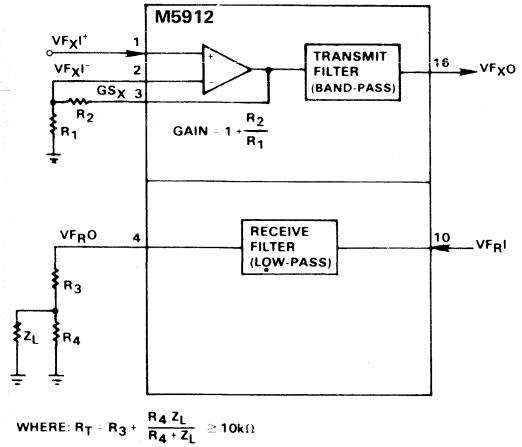
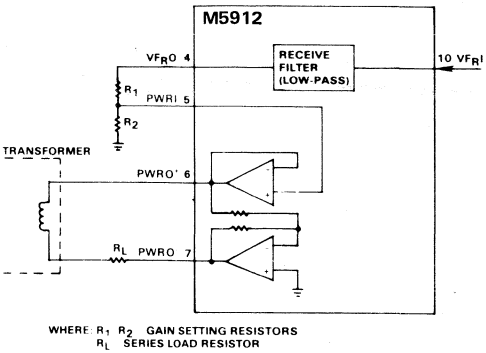


Fig. 3 - Typical connection of the output power amplifier stage



Pins 6 and 7 – PWRO+ and PWRO-

This balanced differential-output amplifier stage is provided to drive low impedance loads directly. The gain of the receive signal may be adjusted by a voltage divider as shown in Figure 3. The series impedance of a load resistor and the bybrid transformer should present an AC load resistance of 600Ω (min.) to the amplifiers in a bridged configuration. With a 600Ω load between pins 6 and 7, the maximum voltage swing across the loads is ±6.4 volts. These may also be used to drive loads which are connected to ground. If the power amplifiers are not required in a particular application they should be deactivated by typing PWRI to V_{BB}.

Pin 8 – V_{BB}

Pin 8 is the negative supply pin. The voltage supplied to this pin should be -5V ± 5%.

Pin 9 – V_{CC}

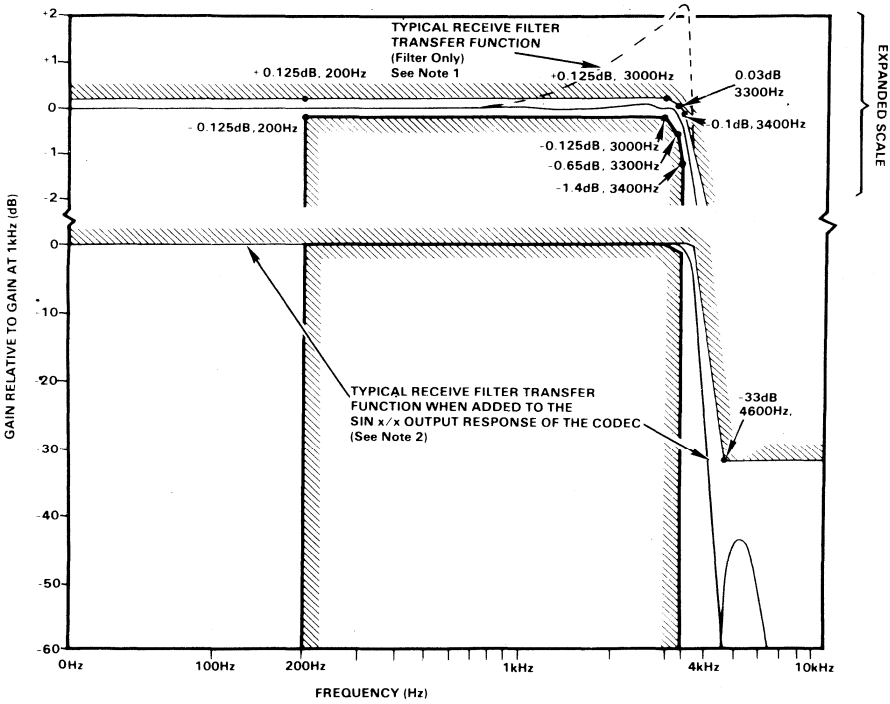
Pin 9 is the positive supply pin. The voltage supplied to this pin should be +5V ± 5%.

Pin 10 – VF_{RI}

Pin 10 is the analog input to the receive filter. The receive signal is typically generated by the decoder section of a μ or A law companding Codec. The receive filter is a low-pass switched-capacitor filter which will pass frequencies up to 3200 Hz and provides the sin x/x correction needed to give the Codec decoder and receive filter pair unity gain over the passband. This filter exceeds the AT&T D3/D4 specifications and is compatible with the CCITT G712 recommendation.
The receive filter transfer characteristics and specifications, including the sinx/x response introduced by the decoder, are shown in Figure 4.

FUNCTIONAL DESCRIPTION (continued)

Fig. 4 - Receive filter transfer characteristics



NOTES:

1. The broken line shows the x/sinx response of the filter only. This response corrects the sinx/x response of the sample and hold output of the codec and provides unity gain in the passband.
2. The Typical filter transfer function shown is the combined response of the codec and the receive filter. The combined response meets the stated specifications.

Pin 11 – GRDD

Pin 11 serves as the digital ground return for the internal clock. The digital ground is not internally connected to the analog ground. The digital and analog grounds should be tied together as close as practical to the system supply ground.

Pin 12 – CLK

The digital clock signal should be supplied to Pin 12. Four clock frequencies (1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.560 MHz) may be used. The desired clock frequency is selected by the CLKS input (Refer to Table 1). For proper operation this clock should be tied to the receive clock of the Codec.

Pin 13 – PDWN

This control input is used to place the M5912 in the standby power-down mode. Power down occurs when the signal on this input is pulled high. Standard TTL levels may be used. An internal pull up to the positive supply is provided. A settling time of 15 ms (typ) should be allowed after power is restored.

Pin 14 – CLKS

The voltage level on this pin will select the desired clock frequency to drive Pin 12. Table 1 defines the clock selection. When using the open circuit (2.560 MHz clock frequency) mode, the capacitance to adjacent signal lines should be minimized.

Table 1 – Input Clock Select

CODEC Clock	Clock Bits/ Frame	M5912 CLK Input Pin 12	M5912 CLKS Input Pin 14
1.536 MHz	192	1.536 MHz	V_{BB}, -5V
1.544 MHz	193	1.544 MHz	GRDD
2.048 MHz	256	2.046 MHz	V_{CC}, +5V
2.560 MHz	320	2.560 MHz	Open Circuit

Pin 15 – GRDA

Pin 15 serves as the ground return for the analog circuits of the transmit and receive sections. The analog ground is not internally connected to the digital ground. The digital and analog ground should be tied together as close as practical to the system supply ground.

Pin 16 – VFXO

Pin 16 is the analog output of the transmit filter. The output voltage range is ± 3.2 volts and the DC offset is less than 200 mV. This output should be AC coupled to the transmit (encoder) section of the Codec.

DECOUPLING RECOMMENDATIONS

PC board decoupling should be sufficient to prevent power supply transients (including turn on and turn on and turn off) from exceeding the absolute maximum rating of the device. A minimum of 1 μF is recommended for each power supply.
A 0.05 μF bypassing capacitor should also be connected from each power supply to GRDA at the M5912 device. However, this decoupling may be reduced depending on board design and performance.

COS/MOS INTEGRATED CIRCUIT

M 22100

4 x 4 CROSSPOINT SWITCH WITH CONTROL MEMORY

- LOW ON RESISTANCE -85Ω TYP. AT V_{DD}= 12V
- "BUILT-IN" CONTROL LATCHES
- LARGE ANALOG SIGNAL CAPABILITY: ± $V_{DD/2}$
- TRANSMITS SIGNALS UP TO 10 MHz
- MATCHED SWITCH CHARACTERISTICS ΔR_{ON}= 5Ω TYP. AT V_{DD}-V_{SS}= 12V.
- HIGH LINEARITY: -0.5% DISTORTION (TYP.) AT 1 KHz, V_{IN}= 5V PEAK TO PEAK V_{DD}-V_{SS}= 10V, R_L= 10 KΩ
- STANDARD COS/MOS NOISE IMMUNITY

The M22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line-to-16-line decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logical one or zero, respectively, to the data input and strobing the strobe input to a logical one. Any number of the transmission gates can be ON simultaneously.
The device is available in 16 lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to	20	V
V_I	Input voltage	-0.5 to V_{DD}	+0.5	V
I_I	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range		100	mW
T_{op}	Operating temperature range: for ceramic	-55 to	125	°C
	for plastic	-40 to	85	°C
T_{stg}	Storage temperature range	-65 to	150	°C

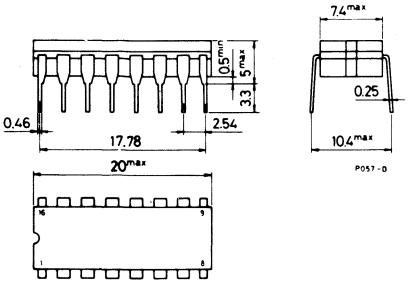
* All voltage values are referred to V_{SS} pin voltage.

ORDERING NUMBERS: M22100 B1 for dual in-line plastic package
M22100 D1 for dual in-line ceramic package frit seal

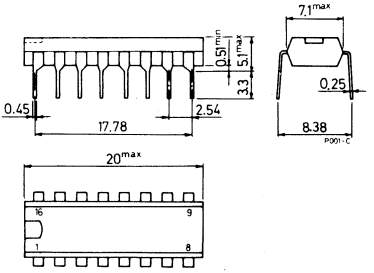
M 22100

MECHANICAL DATA (dimension in mm)

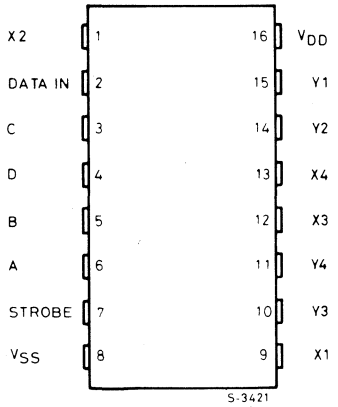
For dual in-line ceramic package, frit seal



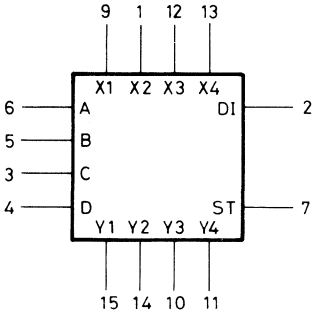
For dual in-line plastic package



PIN CONNECTIONS



FUNCTIONAL DIAGRAM and TRUTH TABLE

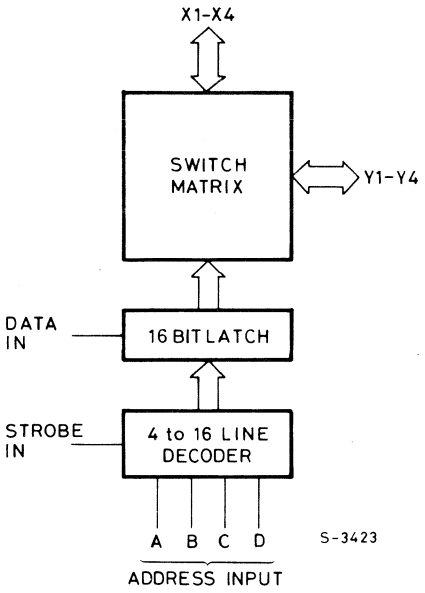


V_{SS} (GND) = 8

V_{DD} = 16 S-3422

Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

LOGIC DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Parameter			Test conditions	V_{DD} (V)	Typical value	Units
I_L	Quiescent supply current		Switches OFF or ON	12	20	nA
I_L	OFF leakage current	Crosspoint	R_L = 10 KΩ		100	pA
R_{ON}	ON resistance				85	Ω
ΔR_{ON}	ΔON resistance				5	Ω
C_{IO}	Feedthrough capacitance				0.2	pF
C_{IS}, C_{OS}	Channel input or output capacitance				30	pF
C_I	Input capacitance				5	pF
	Sine wave response (distortion)		f_{is} = 1 KHz R_L = 10 KΩ		0.4	%
	Feedthrough, crosspoints OFF		f_{is} = 1.6 KHz R_L = 1 KΩ		-95	dB

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C)

Parameter		Test conditions	V_{DD} (V)	Typical value	Units
t_{PHL}, t_{PLH} Propagation delay time	address or strobe	R_L= 10 kΩ C_L= 50 pF	12	200	ns
	input to outputs			20	ns
	across crosspoint			80	ns
t_W Strobe pulse width					

MOS INTEGRATED CIRCUIT

M 36000

PRELIMINARY DATA

64K-BIT READ ONLY MEMORY

- 8K x 8 ORGANIZATION - EDGE ENABLED OPERATION ($\overline{CE}$)
- 250 ns ACCESS TIME, 375 ns CYCLE TIME FOR M36000-4
  300 ns ACCESS TIME, 450 ns CYCLE TIME FOR M36000-5
- SINGLE +5V ±10% POWER SUPPLY
- LOW POWER DISSIPATION: 220 mW MAX ACTIVE
- LOW STANDBY POWER DISSIPATION: 35 mW MAX ($\overline{CE}$ HIGH)
- ON CHIP LATCHES FOR ADDRESSES (CONTROLLED BY $\overline{CE}$ INPUT)
- INPUTS AND THREE-STATE OUTPUTS - TTL COMPATIBLE
- OUTPUT DRIVE 2 TTL LOADS AND 100 pF
- STANDARD 24 PIN DIP (EPROM PIN OUT COMPATIBLE)

The M36000 is a N--channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. This device incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins. The M36000 utilizes a static storage cell with clocked control periphery which allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 35 mW, as compared to unclocked devices which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. The edge enabled operation means greater system flexibility and an increase in system speed, making this device ideally suited for 8 bit microprocessor systems such as those which utilize the Z80. It can offer significant cost advantages over PROM. The M36000 is available in 24-lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS*

V_i	Voltage on any pin with respect to Ground	-1 to +7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature: for ceramic package	-65 to +150	°C
	for plastic package	-55 to +125	°C
T_{op}	Operating temperature	0 to +70	°C

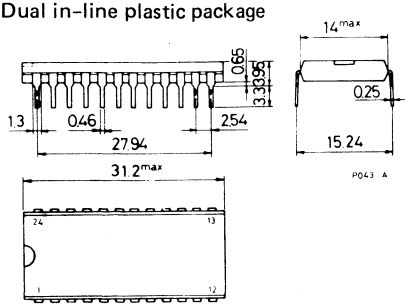
* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS:

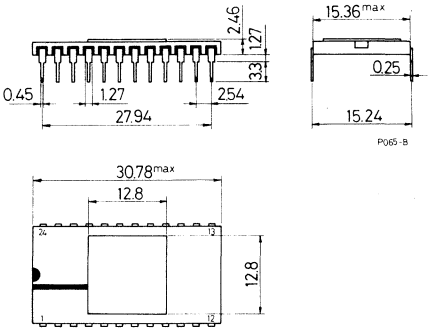
M36000 - 4 B1	for dual in-line plastic package
M36000 - 4 D1	for dual in-line ceramic package
M36000 - 4 F1	for dual in-line ceramic package, frit-seal
M36000 - 5 B1	for dual in-line plastic package
M36000 - 5 D1	for dual in-line ceramic package
M36000 - 5 F1	for dual in-line ceramic package, frit-seal

MECHANICAL DATA (dimensions in mm)

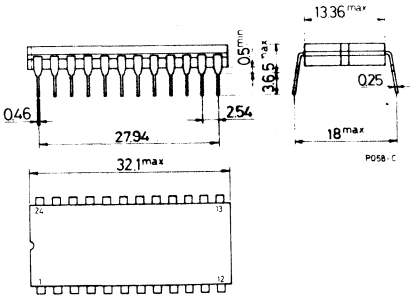
Dual in-line plastic package



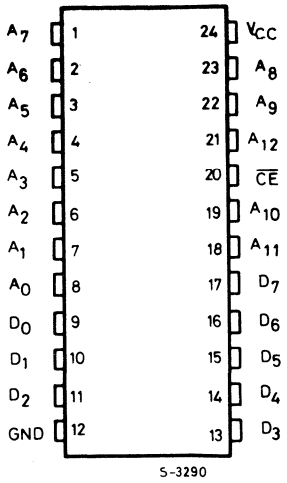
Dual in-line ceramic package



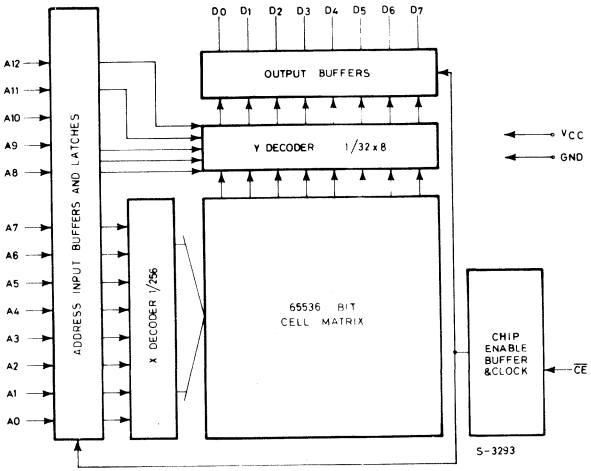
Dual in-line ceramic package, frit-seal



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS[1] (T_{amb} = 0 to 70° C unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	Input high voltage		2		V_{CC}	V
V_{IL}	Input low voltage		-1		0.8	V

STATIC ELECTRICAL CHARACTERISTICS[1] (T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{OH}	Output high voltage	I_{OH} = -220 μA	2.4			V
V_{OL}	Output low voltage	I_{OL} = 3.3 mA			0.4	V
I_{LI}	Input leakage current	V_I = 0 to 5.5V	-10		10	μA
I_{LO}	Output leakage current	Device unselected; V_o = 0 to 5.5V	-10		10	μA
I_{CC1}	Supply current (active)[2]				40	mA
I_{CC2}	Supply current (standby)	$\overline{CE}$ high			8	mA

DYNAMIC ELECTRICAL CHARACTERISTICS[1] (T_{amb} = 0 to 70°C unless otherwise specified)

Parameter		Test conditions	M36000 - 4		M36000 - 5		Unit
			Min.	Max.	Min.	Max.	
t_C	Cycle time	Output load = 2 TTL gate and 100 pF, transition times = 20 ns	375		450		ns
t_{CE}	$\overline{CE}$ pulse width		250		300		ns
t_{AC}	$\overline{CE}$ access time			250		300	ns
t_{OFF}	Output turn off delay			60		75	ns
t_{AH}	Address hold time		60		75		ns
t_{AS}	Address setup time		0		0		ns
t_P	$\overline{CE}$ precharge time		125		150		ns

Notes:

1) A minimum 100 μs time delay is required after the application of V_{CC} (+5V) before propex device operation is achieved. $\overline{CE}$ **must** be at V_{IH} for this time period.

2) Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time.

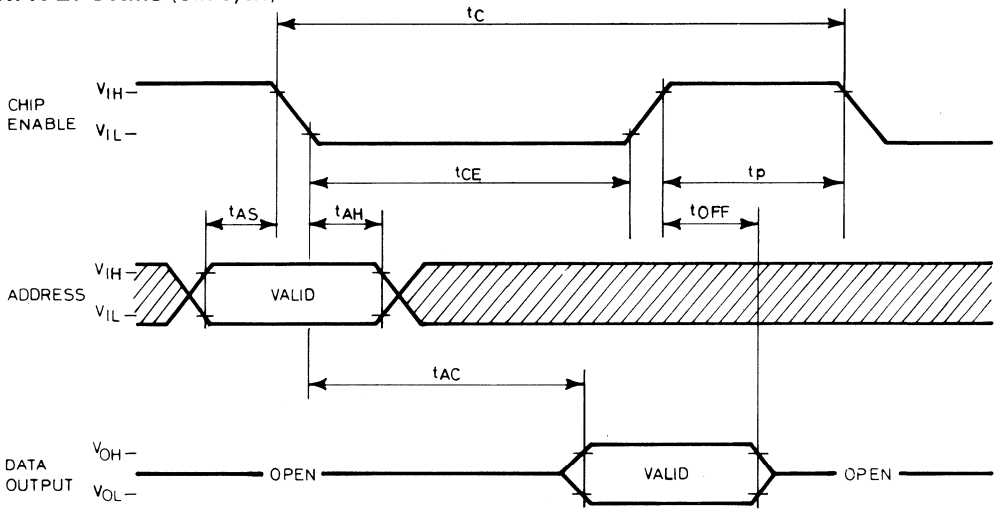
CAPACITANCES (T_{amb} = 0 to 70°C)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	Capacitance measured with Boonton Meter or effective value calculated from: $C = \frac{\Delta Q}{\Delta V}$ with $\Delta V = 3V$		5	8	pF
C_O	Output capacitance			7	15	pF

DESCRIPTION OF OPERATION

The M36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the onchip address registers. New address data can be applied in anticipation of the next cycle once the address hold time specification has been met. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

WAVEFORMS (One cycle)



S-3292

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